A Tri-level Current-Steering DAC Design with Improved Output-Impedance Related Dynamic Performance

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***Abstract* - This paper presents a design of a low-latency 12-bit linear tri-level current-steering digital-to-analogue-converter for use in continuous-time ADCs. The DAC design achieves 12-bit static linearity, while the combination of DAC slice impedance matching with a proposed compensation technique reduces output-impedance related distortion. The technique demonstrates ~10dB improvement in DAC dynamic performance at high frequencies over the Nyquist-band at 100MS/s. The DAC has been verified by simulation results in TSMC 1.2V 65nm CMOS technology.**

***Index Terms*: Tri-level, Current-Steering, DAC, SFDR, HD3.**

I. Introduction

High-performance continuous-time ADC (CT-ADC) architectures as shown in Fig. 1 provide for efficient wideband conversion in applications such as wireless communications. A current-steering DAC (CS-DAC) is a key component of the CT-ADC architecture; consequently a highly linear wideband DAC is necessary to meet the overall ADC specifications. The goal of this work is to design a low-latency high-linearity CS-DAC suitable for a 12-bit CT-ADC architecture as shown in Fig. 1. The top-level components of the CT-ADC are the filter, Flash-ADC (N-bit), DAC (N-bit), integrating-gain-stage and discrete-time (DT) backend SAR-ADC (M-bit). The DAC in this paper is part of a project developing a 100MS/s CT-ADC [1]. In this work, the low latency specification of the DAC is required to match the signal and critical path delays to achieve the wide-bandwidth for the CT-ADC. In order to achieve 12-bit ADC performance using 100MS/s sampling rate, the 5-bit (32-level) unary-weighted CS-DAC must fulfill the following key requirements;

1. The DAC decoder logic must have low latency.
2. The DAC must meet the overall linearity performance requirements of the CT-ADC (i.e. 12-bit).
3. A fully-differential DAC must be suitable for low-voltage (1.2V) and must have low-noise performance.

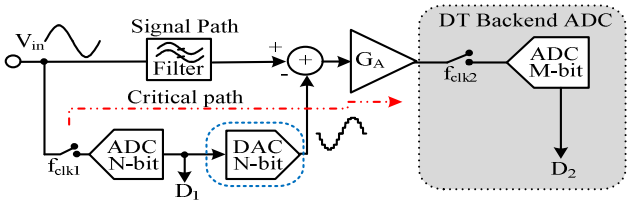

Fig. 1 CT-ADC [1] incorporating the DAC.

The factors in determining the DACs performance in terms of spurious-free-dynamic-range (SFDR) and signal-to-noise-and-distortion-ratio (SNDR) are current-source (CS_{rc}) related mismatch errors [2], switching related timing errors [3], finite-output-impedance of a CS_{rc} [4], and thermal noise due to CS_{rc} [5]. The impact of these errors needs to be minimized in order to achieve good dynamic performance.

The paper is organized as follows: Section II overviews the comparison of the CS-DAC topologies in terms of static-linearity, thermal noise, and output-loading. From this analysis we show why the tri-level DAC (TRI-DAC) topology is chosen for the architecture in Fig. 1. Section III provides the design details of the TRI-DAC blocks such as CS_{rc} slice, bias block and the decoder-logic. The TRI-DAC output-impedance related dynamic performance improvement technique is provided in Section IV. In Section V, the layout discussion and the dynamic performance results of a fully-differential TRI-DAC operating at a 100MS/s sampling rate is presented. Finally, Section VI concludes the paper.

II. CS-DAC Topologies Overview

The following unary-weighted CS-DAC topologies could be employed in the architecture of Fig. 1. a) bi-level DAC (BI-DAC), b) complementary-DAC (CMP-DAC) and, c) tri-level DAC. Equivalent 2-bit differential BI-DAC, CMP-DAC and TRI-DAC implementations are shown in Fig. 2(a), where I_{FS} is the full-scale output current. In this scenario, a BI-DAC CS_{rc} slice is implemented using a 'Sink' device and a constant current offset using a 'Source' device on each current output node. The CMP-DAC and TRI-DAC unit CS_{rc} slice is implemented using 'Sink' and 'Source' devices. However, as compared to the CMP-DAC, the TRI-DAC unit CS_{rc} slice has an extra 'Dump' state, when activated this forms a path between VDD and GND that contributes no current to the output node.

The static-linearity, thermal noise and the code-dependent output loading performance of the CS-DAC topologies is depicted in Fig. 2(b), (c), and (d). The 3-level element selection employed in a unit TRI-DAC exhibits better linearity performance compared to the BI-DAC and CMP-DAC topology for a given level of mismatch and number of bits. This is due to the presence of the 'Dump' state, which forces the output to zero at mid-code. The thermal noise performance of the BI-DAC is poorer when compared to the equivalent CMP-DAC and TRI-DAC implementations, due to the use of offset devices. The CMP-DAC topology does not require fixed CS_{rc} devices; therefore the thermal noise contribution is lower than the BI-DAC. The TRI-DAC

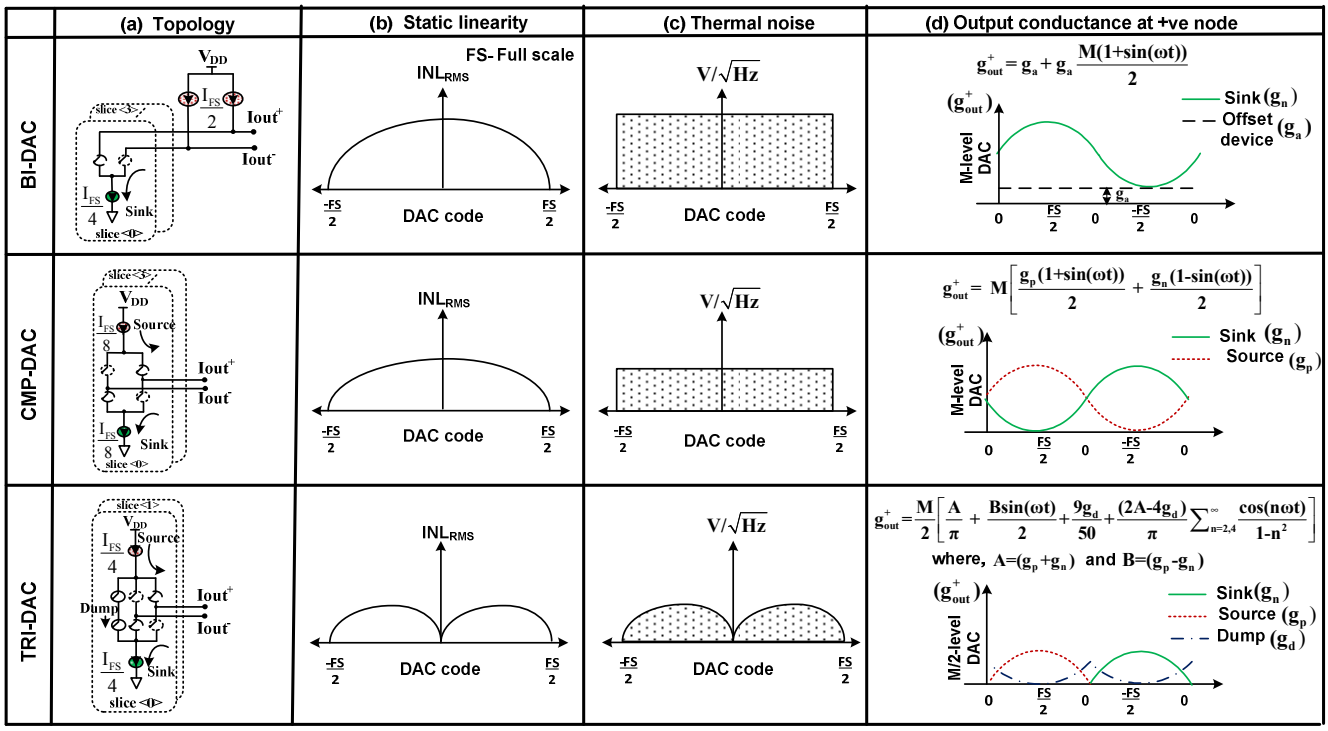

Fig. 2.(a) Unary-weighted CS-DAC topologies and the comparison in terms of (b) static-linearity, (c) thermal noise and (d) output loading.

thermal noise is code-dependent and contributes less noise especially at low signal levels than the CMP-DAC and BI-DAC for an equivalent bit implementation. The three CS-DAC topologies have a code-dependent output loading effect; the load variation at the DAC's positive output node based on an input sine wave is shown in Fig. 2 (d). In the figure, g_n, g_p and g_d are the 'Sink', 'Source' and the 'Dump' mode conductance of a unit CS_{rc} slice respectively. The summation of the output conductance at the output node (±ve node) shows a non-linear effect, which needs to be overcome by impedance matching which is discussed in Section IV. Based on the CS-DAC topologies comparison, a 5-bit unary-weighted TRI-DAC is chosen for the architecture of Fig. 1.

III. TRI-DAC DESIGN

Figure 3 shows a 1.2V 100MS/s 5-bit unary-weighted (33-level/16 CS_{rc} slices) tri-level CS-DAC. In order to evaluate the design, the TRI-DAC's output nodes drive a transimpedance amplifier and the full-scale differential output current is 2.4mA. This amplifier model is implemented with a 45dB gain and a real dominant pole at 100MHz with a 250Ω feedback resistor. The major blocks include the 16x TRI-DAC slices, the bias circuit and the decoder logic, the design of which are detailed in the following sections.

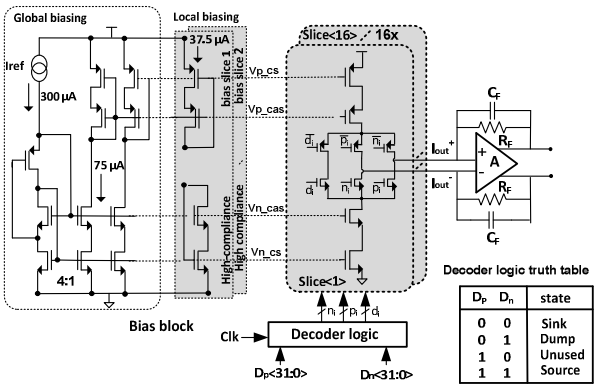

Fig. 3. TRI-DAC top-level architecture.

A. CS-slice

The TRI-DAC consists of 16 DAC slices, such that each slice can simultaneously 'Sink' and 'Source' $75\mu A$ of current, to produce a $150\mu A$ differential step current. The TRI-DAC output nodes drive the 600mV common-mode level of the amplifier. In order to design a 5-bit TRI-DAC for 12-bit linearity with a ±0.5 LSB INL, achieving 99.7% yield, the required relative standard deviation of the unit CS_{rc} [6] can be calculated as

$$\sigma\left(\frac{\Delta I}{I}\right) \le \frac{1}{\sqrt{2^{N+2} * C}} = \frac{1}{\sqrt{2^N}}\frac{0.5}{4.97} = 0.15\%, \qquad (1)$$

where N is the DAC resolution and C is an INL yield related coefficient. To obtain 99.7% DAC yield, C = 4.97. The area of a unit CS_{rc} using the related standard deviation and some technology parameters can be expressed [7] as

$$WL = \frac{1}{2\sigma^2\left(\frac{\Delta I}{I}\right)}\left[\left(\frac{2A_{v_t}}{V_{ov}}\right)^2 + \left(A_\beta\right)^2\right]. \qquad (2)$$

In this work, the overdrive-voltage (V_{ov}) for the n/p CS_{rc} is 300mV and the nMOS $A_{V_T} = 3.8\,\text{mV} * \mu\text{m}$, pMOS $A_{V_T} = 3.4\,\text{mV} * \mu\text{m}$ with $A_\beta = 0.7\% * \mu\text{m}$ for both devices. Using 0.1% standard deviation on both n/p CS_{rc} devices, the initially estimated gate area is 345 μm^2 and 288 μm^2 respectively. The (W/L) ratio of the n/p CS device is determined in such a way that it maintains the required standard deviation and the overdrive voltage on both the devices. Using different (W/L) ratios for the n/p CS_{rc} device, the SPICE-level DNL, INL results are obtained.

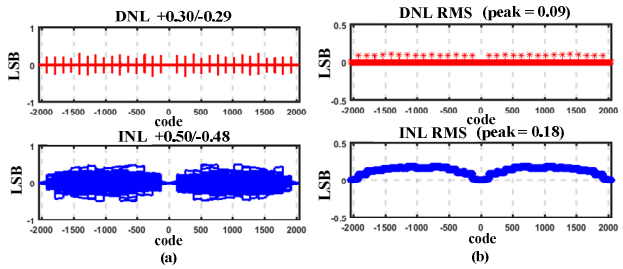

Fig. 4. TRI-DAC DNL/INL results at 12-bit level using 100 MC runs.

Using device aspect ratios of 32/10 μm and 80/4 μm for the n/p CS_{rc} device respectively; the values obtained for $\sigma(\Delta I_n/I_n)$ and $\sigma(\Delta I_p/I_p)$ are 0.12% and 0.13% respectively. The TRI-DAC top-level DNL and INL performance results using Monte-Carlo (MC) simulations seen in Fig. 4(a) show the DNL/INL is $\leq$0.5 LSB. The observed maximum DNL_{RMS} and maximum INL_{RMS} are 0.09 LSB and 0.18 LSB respectively as shown in Fig. 4(b).

B. Bias block and decoder logic

The proposed bias circuit is shown in Fig. 3. The biasing circuit is divided into two parts "Global biasing" and "Local biasing". The global biasing uses $300\mu A$ of the reference current and a current of $75\mu A$ flow through each parallel branch. Low-voltage-threshold (LVT) devices are used to implement the biasing circuit to overcome the voltage headroom limitations. A reference branch is designed using 4x larger devices than its replica branches to reduce the effect of mirrored noise. Additionally, the local biasing is divided into two high compliance bias slices for a better layout and symmetry. To satisfy the 'Sink', 'Source' and 'Dump' mode operation in a unit CS_{rc} slice; the TRI-DAC decoder logic is simply implemented using 2-input NAND gates interfaced directly to the latch outputs in the 5-bit Flash-ADC. The decoder logic truth table is shown in Fig. 3. In this design, the use of a simple thermometer-decoded input stage minimizes element transitions and is helpful in reducing dynamic distortion effects such as ISI [8].

IV. Output-Impedance Related HD3

The signal-dependent finite-output-impedance of a CS_{rc} causes distortion in fully-differential DACs which degrades the SFDR/HD3 performance at high frequencies. The code-dependent output-conductance behavior of the TRI-DAC differs significantly from the BI-DAC and CMP-DAC topology as shown in Fig. 2(d), due to the 'Dump' mode. In an N-bit and M-level thermometer decoded TRI-DAC, if k is the number of CS_{rc}'s that are turned 'ON' for a given input-code, then there will be $(M/2-k)$ number of CS_{rc}'s operating in a dump mode. The TRI-DAC code-dependent output-conductance variation for sinusoidal input-signal at the positive output node is shown in Fig. 2(d). Intuitively, it can be observed from the figure that g_n, g_p and g_d should be made equal to remove the code- dependent output-conductance variation in a TRI-DAC unit CS_{rc} slice.

In this work, the TRI-DAC unit CS_{rc} slice (uncompensated) is initially designed with an n/p section output impedance of 0.91MΩ and 1.94MΩ respectively. The dynamic performance results of the uncompensated

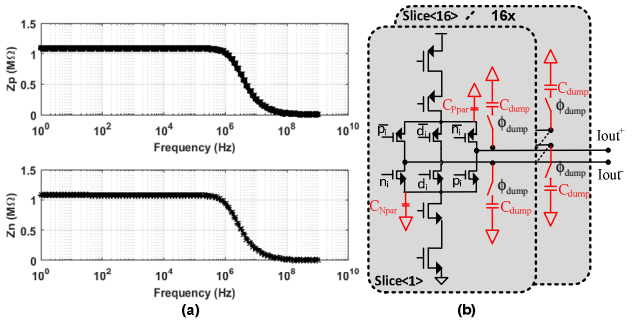

Fig. 5(a) n/p section output-impedance, (b) TRI-DAC slice design using capacitive compensation.

TRI-DAC slice is discussed in Section V. To improve the HD3/SFDR performance, impedance matching between the n/p sections in a unit CS_{rc} slice is employed. The matched n/p section output impedance is 1.08MΩ and 1.10MΩ respectively as shown in Fig. 5(a). The impedance matching between the n/p sections can be realized by tuning the device sizes of the cascodes and the switches of both the sections without disturbing the CS_{rc}'s. Even though the n/p section impedance matching is employed; the output nodes of the TRI-DAC still has a code-dependent variable output loading effect due to the 'Dump' mode. The output capacitance of a switched 'ON' TRI-DAC unit CS_{rc} slice is approximately 70fF at both the output nodes. The 'Dump' state contributes no current to the output node; hence the capacitance seen at the output node is zero. Therefore for 16x TRI-DAC slices; loading can vary from 0 to 1.12 pF for the minimum and maximum input-code respectively. This signal-dependent capacitance causes distortion in the TRI-DAC and deteriorates its dynamic performance at high frequencies.

A technique in [9] used capacitors between the latch and CS_{rc} switch devices to reduce the code-dependent load effect causing dynamic glitch variation in a binary-weighted DAC. Our proposed solution adds a switch $\emptyset_{dump}$ in each DAC slice to the output nodes in 'Dump' mode so that the capacitive loading becomes C_{dump} as shown in Fig. 5(b). The dump capacitor is implemented using an n/p device to mimic the CS_{rc} device parasitic capacitance. The aim is to equalize the DAC capacitive loading for all input codes. This technique helps to improve HD3/SFDR by ~10dB at high frequencies as shown by the results in Section V.

V. Layout and Simulation Results

The TRI-DAC layout size is 176μm x 372μm, including 16x DAC slices, bias circuitry and decoder-logic as shown in Fig. 6. Each of the 16x slice strips consist of n/p CS_{rc} device, cascodes and switch devices which has an outline of 163μm x 14μm and maintains the symmetry along its horizontal axis. The TRI-DAC slice strip contains shorter dummy devices to help with matching and to reduce the shallow-trench-isolation (STI) effects. The local bias section is placed at either side of the 16x DAC slice strip array and connects to the global bias block. The layout includes dummy devices matched to the n/p sensitive devices in each slice. The layout consists of dedicated routing channels to reduce parasitic capacitance and to minimize IR power drop

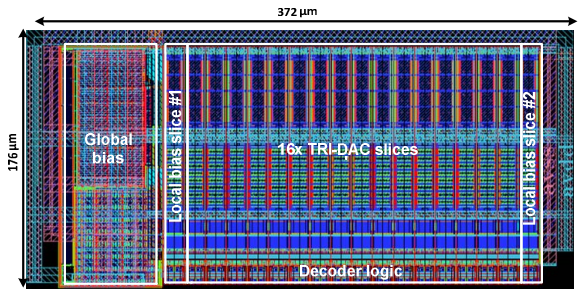

Fig. 6. Layout of the TRI-DAC

across the full design. The decoder logic in each DAC slice is driven by a separate digital 1.2V supply and isolated rings to minimize the supply noise interference.

The output swing is 1.2V peak-to-peak differential into a 250Ω feedback resistor of a transimpedance amplifier with a full-scale output current of 2.4mA. The power consumption from the blocks including bias, 16x TRI-DAC slices and the decoder logic is 2.55mW. The TRI-DAC extracted simulations show DNL, INL below ±0.5 LSB and the transient simulations show a full-scale settling time of 354.63ps including a 28.11ps driver delay.

In order to assess the dynamic performance, the 5-bit MSB TRI-DAC is combined with an ideal 7-bit binary-weighted LSB DAC. The design drives an amplifier model at the output stage as described in Section III to observe the performance differentially. Fig. 7 shows the SNDR/SFDR with respect to the signal frequency over the Nyquist range using a sampling rate of 100MS/s

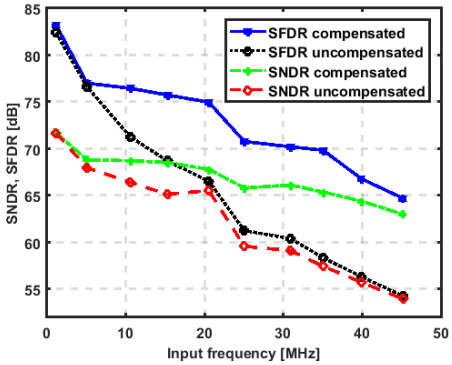

Fig. 7. SNDR/SFDR versus input-frequency for uncompensated and compensated TRI-DAC.

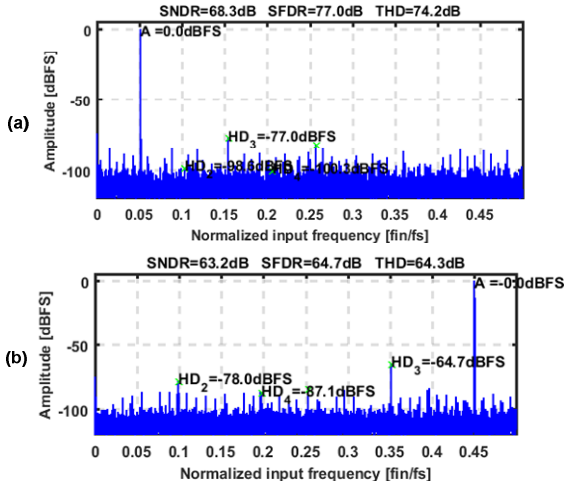

Fig. 8. FFT spectrum for input-tones at (a) 5.13MHz (b) 45.05MHz.

The SNDR/SFDR performance for the uncompensated TRI-DAC is seen to degrade significantly with increasing frequency. However, using the combined n/p impedance matching and capacitive compensation technique, the DAC shows improved SNDR/SFDR performance over the Nyquist band, particularly at higher frequencies. Fig. 8(a) and 8(b) shows the Fast-Fourier-Transform (FFT) spectrum for the input tones at 5.13MHz and at 45.05MHz respectively, for the compensated TRI-DAC running at 100MS/s. The SNDR/SFDR at 5.13MHz and 45.05MHz are 68.3/77.0dB and 63.2/64.7dB respectively.

VI. Conclusion

In this work, a TRI-DAC topology is chosen for its static-linearity and thermal-noise performance benefits over the BI-DAC and CMP-DAC topology. The proposed TRI-DAC achieves 12-bit static-linearity and low latency i.e. 354.63ps settling time. The TRI-DAC is seen to have a code-dependent output loading effect, which mitigates against its thermal noise and mismatch performance design advantages. The compensation technique proposed in this work minimizes this non-linear loading effect and improves the output-impedance related dynamic performance of the TRI-DAC over the Nyquist-band.

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