A Study into the Electrical Trim of Silicon Chromium Thin Film Resistors

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Declaration

This thesis is presented in partial fulfilment of the requirements of the degree of Doctor of Philosophy at the University of Limerick.

It is entirely my own work and has not been submitted to any other higher education authority nor for any other academic awards in the University.

Where there has been use made of the work of others, it has been fully acknowledged and referenced.

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Fergus Downey

May 2014
Dedication

I dedicate this thesis to my mother, Mary.
Acknowledgements

First I have to thank my fiancée Emer, who has always supported me and sacrificed our time to allow me complete this thesis. Her encouragement and kindness were always there when I felt disheartened and motivated me to continue on. I also thank my parents for their inspiration which lead me to continue my education towards a PhD.

I started the PhD process while working in the Reliability group in Analog Devices Limerick. During my five years there I worked on a huge amount of projects that gave numerous options for a research project. James Molyneaux mentored and supported me in starting a post graduate research program and focused me towards a suitable and achievable project. I had a great time working in Reliability and have to thank James, John, Mark, Marion, Colm, Mary, Rob and Stephanie who were always available to provide great advice and help me out.

Three years ago I moved to the precision DAC group in Analog Devices Edinburgh design centre. While changing career from reliability to design in the middle of the PhD process did not free up any more of my personal time, it was a job I had discovered through the PhD process which I desired to pursue. Roddy McLachlan not only provided me with the opportunity in design but also provided the questions that are key to this thesis. I would like to thank Roddy and the other members of the Edinburgh design centre who were always available to answer my questions and tolerated my messy test setup in the lab.

Finally I would like to acknowledge and thank my PhD supervisor and mentor Ian Grout. Over the last six years Ian has always gone out of his way to guide me through the PhD process. Even after six years, I was always encouraged with my progress after meeting Ian.

Without the support of all those mentioned above I would have abandoned the PhD years ago. Looking at the finished thesis now I still cannot believe it is complete.
Abstract

A Study into the Electrical Trim of Silicon Chromium Thin Film Resistors

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Silicon Chromium (SiCr) Thin Film Resistors (TFRs) have been developed and integrated into CMOS ICs for over twenty years. Current state of the art sputtering technology achieves integrated resistors with temperature coefficient of resistance (TCR) of -25 ppm/°C and absolute resistance values post LASER trim of 0.01%. Discrete passive resistors however are now stating TCR figures of 0.05 ppm/°C which vastly improves the stability of the resistor over temperature. Discrete resistors achieve these accuracies by designing a specific substrate that compensates for the TCR of the resistive film.

This dissertation details the implementation of a novel TCR and absolute resistance post processing trimming technique (iTrim). This trimming method results in TCRs and absolute resistance values equivalent to discrete resistors but integrated into a standard CMOS IC stack. iTrim is a controlled Joule heating technique, generated using high power densities to precision anneal the SiCr film post processing. The energy generated from Joule heating induces a physical change to a portion of the resistive film. The altered film is Chromium dominant which results in a lower resistance and positive TCR. By balancing the ratio of standard negative TCR material and new positive TCR material, a near zero TCR resistor can be generated. The ratio of positive TCR material to negative TCR material is measured and controlled using a power sweep across the resistor. From this power sweep, the power coefficient of resistance (PCR) can be extracted. The PCR value has been shown to provide an efficient approximation of the TCR value while only requiring single ambient temperature testing.

In the first section of this thesis an overview is given of current integrated resistor technologies. In the second section a detailed study is carried out on pre and post trim SiCr resistors. The final section reviews a test chip with an integrated 10 kΩ resistor that uses iTrim to trim the TCR to less than 3 ppm/°C and the absolute resistance to 0.02%.
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1. Introduction

Resistors are one of the most important devices used in any electrical circuit. Resistors are used to quantify the relationship between the flow of charge through, and the potential energy across, a resistive element. This relationship is defined as Ohm’s law and is arguably the most important and well known of all electrical equations. Ohm’s law was defined by George Simon Ohm and presented in his 1827 work "The Galvanic Circuit Investigated Mathematically" [1].

\[ V = IR \]

Ohm’s law is used by circuit designers to calculate required resistances to achieve the specific requirements of an electrical circuit. For example, this can be as simple as the design of a resistor divider where the chosen resistor values determine the power consumption, output voltage and output noise. As the requirements for higher precision circuits increased, designers realised the difficulty in achieving a high accuracy absolute resistance value from resistors produced on non-ideal fabrication processes and operating in a range of environments. This demand has driven research on how the electrical properties of a resistor change with temperature, applied current and voltage. Combining these parameters and sensitivities, leads to a more complex appreciation of a resistor. In the 1920’s, this improved understanding resulted in engineers such as Manfred von Ardenne creating the concept of an integrated circuit with the introduction of the Loewe 3NF three stage RF amplifier [2]. The 3NF three stage amplifier was the first to integrate the two capacitors and four resistors along with the three triodes in a single glass tube. The resistors consisted of tubes with carbon coated glass rods. The 3NF valve can be seen
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incorporated into the 333 radio receiver in Figure 1-1 along with an optical image of a carbon coated resistor.

![Image of 333 radio receiver with integrated resistors in the 3NF Multi-valve](image)

Figure 1-1: The 333 Radio Receiver with integrated resistors in the 3NF Multi-valve taken from Loewe AG [3] and a picture of a carbon coated resistor [4].

With the entry of the silicon age, there was continued demand for improved precision in resistor absolute value. This requirement for precision competed with a desire to integrate the circuit components together on a small substrate surface area and in a cost efficient manner. This led to Jack Kilby achieving the integrated circuit, comprising of resistors, transistors and capacitors on a single substrate as detailed in his 1959 patent application [5]. It took another ten years of using precision external resistor arrays before processing had developed to a point where integrated resistors were accurate enough to meet the more stringent demands of the time. This was accomplished by Dooley in 1971 with the creation of a fully integrated 6 bit digital to analogue converter (DAC) [6]. This DAC comprised of an array of diffused resistors. A diffused resistor is a heavily doped tub in the silicon substrate. The geometry of the resistor is defined by the length and width of this tub. To this day, the challenge has been to achieve the precision of a standalone resistor with the compact volume of an integrated circuit. Modern CMOS processes contain a variety of resistor types which are suitable for various applications. The most advanced of these are Silicon Chromium (SiCr) thin film resistors (TFRs) which are extremely uniform in terms of electrical and thermal properties.
Although SiCr resistors are the best integrated resistors available, absolute resistance tolerances post fabrication are still found to be greater than 1% of the target resistance value. To reduce the absolute resistance tolerance trimming is required. The most accurate commercially available trimming method is LASER trimming which can achieve tolerances of 0.01% [7]. This minimum tolerance matches the best discrete resistor absolute values [8]. The stand alone or discrete resistor is superior in terms of sensitivity to temperature, voltage and current density resulting in a more stable and reliable resistor. This presents a need in the semiconductor industry for a method to achieve an accurate integrated resistor that is stable across temperature and voltage ranges for high precision applications. The novel trimming method presented in this thesis aims to meet these high precision requirements using technology currently available to most analog integrated circuits (IC) manufacturers. This new trimming method can trim a number of resistor related specifications that produces an overall superior integrated resistor. In this Chapter, a review of current technologies and classification for standalone and integrated resistors is presented. Also advanced trimming techniques are explained along with an introduction to the novel trimming technique called ITtrim.
1.1. Resistor Technology and Classification

As mentioned in the introduction, there is a broad history in resistor development. Technology variations exist to meet a range of electrical requirements and budgets. Each application prioritises one requirement over another in order to meet product precision requirements while reducing cost through widening of limits for less critical specifications. The main figures of merit interesting a system designer for a resistor are as follows:

- Resistance value
- Resistor value absolute tolerance
- Resistor value matching tolerance
- Temperature coefficient of resistance (TCR)
- Power coefficient of resistance (PCR)
- Voltage coefficient of resistance (VCR)
- Noise
- Power rating
- Temperature rating
- Load life stability
- Cost

When choosing a resistor technology it is important to understand these parameters and how they interact across temperature and load in order to guarantee functionality in the products final operating environment. Selection of inadequate or lower performance resistors will have diminishing performance effects on the connected circuitry such as precision operation amplifiers (Op-Amp), voltage references or data converters. The following sub sections will introduce the reader to these criteria and briefly examine the performance of major resistor types in relation to these specifications in order to understand what is expected of a precision component.
Chapter 1: Introduction

1.1.1. Resistor absolute value and tolerances

A resistor absolute value may be in the range of a 0 Ω current shunt resistor to greater than 20 billion Ohms (GΩs) for high voltage applications. The absolute resistance tolerance depends on the performance needs of the electrical circuit. It is extremely difficult to produce a resistor with an absolute resistance tolerance below 1% post fabrication. Trimming can be used post processing to reduce the absolute tolerance to below 0.01% for resistor absolute values of between 10 Ω and 10 MΩ [9]. For lower value resistors of less than 1 Ω, tolerances of only 0.1 % are achievable post trim mainly due to the area required for low resistance values [10]. A large initial area is required to guarantee that with process variations the required absolute value is always greater than the highest absolute value post fabrication. This is because LASER trimming involves the removal of material which results in an increase of resistance. If the post fabrication resistor has a greater absolute resistance than the target value, plus allowable tolerance, the trimming process will not be capable of reaching the desired absolute value.

For circuit configurations such as Op-Amps, resistance matching or tracking between resistors is more important than the absolute tolerance of the resistor. This is because the resistors in these IC’s are configured as a voltage divider. The output voltage is related to the ratio of the series resistors rather than the absolute value. In this situation high matching achieved through close proximity of processed resistors will give much better results than two separately processed resistors trimmed to match. To achieve good matching between resistors, the best choice is commonly to purchase a resistor network where the desired resistors are located on the same device. For the LT5400 matching of 0.01 % between the resistors absolute values can be achieved [11].

1.1.2. Temperature coefficient of resistance (TCR)

The major resistor sensitivity is to temperature and is represented by industry as the temperature coefficient of resistance or TCR of the resistor. This value, measured in parts per million per Degree Celsius (ppm/°C), is usually found to be a positive value indicating a linear resistance increase with temperature. In applications were a precision resistor has to operate over a large temperature range, the resistance variation due to the
TCR can be much greater than the initial absolute tolerance of the resistor. Metals are an example of a material that has a positive TCR. This is due to the increased carrier scattering that occurs with temperature rise. A negative TCR can be induced in some materials by the thermal expansion of the film with temperature. In this case, as the ambient temperature increases, the resistive material will also increase in size resulting in the conductive crystals in the resistive film moving apart. As the crystals separate the number of electrons conducted between crystals by a tunnelling process increases. As detailed in Chapter 2 Section 2.4, the rate of electrons tunnelling increase with temperature resulting in a negative TCR.

A resistor with low TCR can be produced by balancing a negative TCR with a positive TCR. Vishay successfully does this with their foil resistors [12]. The foil is a Zeranian film deposited on a hard epoxy substrate. As temperature increases the Zeranian foil has a +10 ppm/°C TCR but the Zeranian film also has a large coefficient of thermal expansion. This would result in a large negative TCR if not for the hard epoxy which restricts the films expansion. The TCR resulting from the restricted film expansions is then limited to approximately -10 ppm/°C. The negative and positive TCRs largely cancel each other out and the actual Zeranian film is found to have a TCR of less than 1 ppm/°C [13]. In applications such as resistor dividers, if both resistor’s TCRs are equivalent, the ratio between the resistors will remain constant over temperature. In this circumstance, a resistor’s individual TCR is not as important as the overall tracking between the resistor’s TCR values. Equation 1-2 gives the standard formula for TCR calculation. For polynomial fits, this relationship is represented by two terms in more accurate resistor models.

\[
TCR = \frac{R_1 - R_2}{R_1} \frac{10^6}{T_1 - T_2} (ppm/°C)
\]

\(T\) is the ambient temperature at which the resistance measurement was performed and \(R\) is the resistance of the resistor.
1.1.3. Power and Voltage Coefficients of Resistance

Temporary modification of the absolute resistance value is not only caused by ambient temperature change but also by the applied electrical bias. The voltage coefficient of resistance (VCR) and the power coefficient of resistance (PCR) measure the non-linearity of the resistor related to the electrical bias. VCR is connected to higher intensity electric fields generated with an increase in voltage. The electric field affects the random motion of defects, such as vacancies, usually resulting in a lower resistance [14] [15] but sometimes resulting in an increase in resistance [16]. The PCR is tied to the TCR of the device due to self-heating. As power increases across a resistor, self-heating ensues. This self-heating leads to thermal gradients across the resistive film which gives variations in the sheet resistance due to the TCR of the material. VCR is measured by applying a high frequency and high amplitude square wave signal across the resistor [17]. The fast transient signal avoids any self-heating as there is not enough time for the resistor to thermally stabilise. Therefore, any change in resistance found during the characterisation is a direct result of the increase in voltage. A basic VCR calculation can be made using equation 1-3. VCR is a concern in applications such as pulse width modulated (PWM) outputs where the fast transients can affect the absolute value of any series resistors.

\[
VCR = \frac{R_1 - R_2}{R_1} \cdot \frac{10^6}{V_1 - V_2} \text{ (ppm/V)}
\]  

1-3

PCR is measured by applying a longer pulse to allow the film to heat up and reach a steady state junction temperature. Any change in resistance caused by the longer voltage pulse, including any VCR related change, can be used to calculate the PCR. The formula for PCR is given in equation 1-4.

\[
PCR = \frac{R_1 - R_2}{R_1} \cdot \frac{10^6}{W_1 - W_2} \text{ (ppm/W)}
\]  

1-4

In an application such as current sensing, the PCR can give non-linear voltage potentials across the resistor as the rising current heats the resistive film. It is therefore
important for a shunt resistor to have a low PCR, high heat capacity and thermally conductive substrate to regulate the generated heat.

1.1.4. Resistor Noise

When a potential is applied across any resistive material, noise is generated by the random motions of the charge carriers traveling through the film. This noise amplitude can be found to have a Gaussian distribution which can be measured by using the root mean square, 1-5.

\[ v_n = \sqrt{v^2} \text{ (V)} \] 1-5

Some noise sources are dependent on frequency. These noise sources have a spectral shape which can be measured using the noise power spectral density function, 1-6.

\[ S_v(f) = \frac{v_n^2}{\Delta f} \left( \frac{V^2}{Hz} \right), \quad f \geq 0 \] 1-6

The noise power spectral density can be interpreted as the noise power in a 1-Hz bandwidth. There are many different types of electrical noise related to the electron flow. These include thermal noise, flicker noise, shot noise, generation-recombination noise and popcorn noise. For resistors, the primary sources of noise are thermal noise and flicker noise [18]. The sum of these noise sources under defined conditions and electrical bias will provide the total noise for the system. Thermal noise is caused by thermal random motion or Brownian motion of charge carriers [19] [20]. As temperature and/or resistance increases these random motions are amplified leading to a rise in noise levels. The spectral density of this spatially distributed motion in a resistor is measured using equation 1-7.

\[ S_v(f) = 4kTR \left( \frac{V^2}{Hz} \right), \quad f \geq 0 \] 1-7
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Flicker noise or $1/f$ noise is currently believed to be caused by the random trapping of charges in the surface interface of the resistive material and the surrounding electrical insulator [21] [22]. These trapped charges lead to charge mobility fluctuations along this interface. The combinations of these actions give a noise spectrum which varies with $1/f^{\alpha}$ where $\alpha$ has been found to be close to unity. Flicker noise is the dominant noise at low frequencies due to $1/f$ relationship with frequency.

![AD5791 noise spectral density versus frequency](image)

**Figure 1-3: AD5791 noise spectral density versus frequency [23].**

Figure 1-3 shows the noise spectral density versus frequency for the AD5791. The AD5791’s output noise is dominated by the noise from the SiCr resistor used in the segmented R2R DAC. The AD5791 has an output impedance of 3500 Ω which results in a thermal noise of $7.5 \text{ nV} / \sqrt{\text{Hz}}$ and a $1/f$ noise of up to $50 \text{ nV} / \sqrt{\text{Hz}}$ at a frequency of 0.1 Hz.
1.1.5. Resistor Reliability

Reliability of a resistor needs to be accounted for once the minimum initial performance requirements of the resistor are defined. The reliability of the resistor is defined as the stability of the absolute resistance value over the operational lifetime of the resistor. Typical operational lifetimes for electronic components are required to reliably operate for a period of 10 years in a temperature range of -40 °C to 85 °C. To meet this requirement, device manufacturers stress individual components in order to understand and model the performance degradation. These models are then used to extrapolate lifetimes for the devices operating under nominal conditions based on short term lifetimes under stress conditions. Failure modes associated with resistor failure are thermo-migration [24], electro-migration [25], mechanical stress and oxidation [26].

Thermo-migration occurs when the atoms contained within the resistive film gain enough energy, generally called activation energy, to break from their bonds and move to a cooler point along the thermal gradient [24]. As more atoms move, a void will start to form leading to an open circuit.

Electro-migration is caused by the electric field, generated by the electron flow, pulling atoms from their bonds, at the cathode end of the resistor, and depositing the atoms at the anode [25]. Electro-migration is accelerated with higher temperatures as the bonds become easier to break.

Stress migration is induced when regions of high stress and low stress exist on a structure. Atoms will move along the stress gradient from high to low stress areas resulting in an open circuit [26]. Stress migration can also be caused by thermal change as the surrounding materials of the resistor may have different thermal expansion coefficients. Oxidation can be caused by the resistive element being exposed to air or to humidity. This oxidation changes the composition of the film which can reduce or increase the resistance [26]. It can also make the film more susceptible to the failure mechanisms mentioned previously. By modelling these failure modes, manufacturers can specify maximum power ratings over a given temperature range to guarantee the user a defined stability for resistance related parameters over the required operational life span.
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1.1.6. Resistor Overheads and Cost

A decisive factor in choosing a resistor technology can be the cost. For external resistors, cost not only covers the purchase price of the resistor but also the cost of mounting the resistor to the PCB board, the area of PCB required to take the resistor and the cost of time required to test and inspect the mounted resistor. Where feasible, it is preferred by system manufacturers to have the passive components integrated into the IC and therefore reduce the amount of passives on the PCB. There is a cost implication for IC manufacturers to integrate these components, especially for high precision resistors. These high precision resistors are usually fabricated on expensive processes and require extra masks and processing steps compared to the base process. IC manufacturers will consider integration as a cost efficient method if system manufacturers are unable to mount an equivalent external resistor at an equivalent cost. This generally is not the case as the best external resistors currently outperform their integrated rivals.

1.2 Integrated and Discrete Resistors

In the previous sections of this Chapter, a brief overview of important resistor parameters was presented. This section will give examples of various resistor types and their respective advantages in terms of performance parameters. Table 1-1 and Table 1-2 provide ratings for a selection of both external and integrated commercially available precision resistors. For the discrete resistor table, the cost of the detailed resistors has been added to highlight the price a systems manufacturer will pay to attain the performance of these precision resistors. For the integrated resistor table, a selection of data points has been collected from literature to allow a comparison with the discrete solutions. The integrated resistor data points demonstrate the variability in electrical performance for various recipes.
### Table 1-1: Precision discrete resistors.

<table>
<thead>
<tr>
<th>Resistor Type</th>
<th>Resistance Range (Ω)</th>
<th>Absolute Tolerance Post trim (%)</th>
<th>Absolute TCR (ppm/°C)</th>
<th>PCR (ppm/W) And/or VCR (ppm/V)</th>
<th>Power rating (W)</th>
<th>Temperature range (°C)</th>
<th>Lifetime (hours)</th>
<th>Cost (USD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wirewound [30]</td>
<td>0.1 to 55 M</td>
<td>0.01</td>
<td>10</td>
<td>-</td>
<td>2</td>
<td>-55 °C to 145 °C</td>
<td>-</td>
<td>$ 6.6 [27]</td>
</tr>
<tr>
<td>NiCr [31] [32]</td>
<td>10 to 200 M</td>
<td>0.01</td>
<td>5</td>
<td>0.01 ppm/V</td>
<td>2</td>
<td>-55 °C to 155 °C</td>
<td>8000</td>
<td>$ 4.8 [28]</td>
</tr>
<tr>
<td>Bulk Metal Foil [33]</td>
<td>5 to 1 M</td>
<td>0.001</td>
<td>0.2</td>
<td>5 ppm/W</td>
<td>2.5</td>
<td>-55 °C to 125 °C</td>
<td>2000</td>
<td>$ 40 [29]</td>
</tr>
</tbody>
</table>

### Table 1-2: Precision integrated resistors.

<table>
<thead>
<tr>
<th>Resistor Type</th>
<th>Sheet Resistance (Ω/□)</th>
<th>Absolute Tolerance Post trim (%)</th>
<th>Absolute TCR (ppm/°C)</th>
<th>PCR (ppm/W) And/or VCR (ppm/V)</th>
<th>Current rating (mA/µm)</th>
<th>Temperature range (°C)</th>
<th>Lifetime (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-silicon</td>
<td>330-1500 [41] [42] [37]</td>
<td>0.015 [40]</td>
<td>590 [36]</td>
<td>-25 ppm/V [36]</td>
<td>0.5 [34]</td>
<td>-40 °C to 110 °C</td>
<td>10000 hours</td>
</tr>
<tr>
<td>NiCr</td>
<td>20-200 [18]</td>
<td>0.01 [18]</td>
<td>25 [38]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SiCr</td>
<td>100-2000</td>
<td>0.01</td>
<td>25</td>
<td>400,000 ppm/W</td>
<td>&lt; 0.2</td>
<td>-40 °C to 125 °C</td>
<td>10000 hours</td>
</tr>
<tr>
<td>TaN</td>
<td>25-125 [18]</td>
<td>0.01 [18]</td>
<td>100 [39]</td>
<td>-</td>
<td>2.75 [35]</td>
<td>-40 °C to 125 °C</td>
<td>100000 hours</td>
</tr>
</tbody>
</table>
1.2.1 Discrete Resistors

Precision external resistors are used in applications such as current sense and current to voltage conversion where integrated resistors are unable to meet operational requirements. In these applications typical values for TCR are below 5 ppm/°C with absolute resistance tolerance values below 0.1%. In applications when the requirement for precision dominates cost, foil resistors are ideal to guarantee performance specifications. Various forms of available precision resistors are listed below.

- Wirewound resistors are used due to their low noise and reliability. The limits of these resistors are caused by electrical stability issues due to the high inductance of the coil and the physical size of the package. Wirewound resistors are ideal in high precision, low frequency applications which can tolerate the extra space requirement for the bulky package [30].

- Thin film resistors comprise mainly of the materials nickel chromium (NiCr) and SiCr. Both materials can be biased with high power densities and have low VCR and TCR effects. These resistors are the most widely used when precision is required but at an affordable cost [32].

![Figure 1-4: Construction of a Vishay foil resistor. Taken from Resistor Theory and Technology [18].](image)

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A cross section of a Vishay foil resistor can be seen in Figure 1-4. Zeranian foil resistors dominate when it comes to performance requirements. The high thermal conductivity and homogeneous structure of the material in combination with LASER trimming make this resistor type the most precise but also most costly of all fixed discrete resistors. [13] [33].

### 1.2.2 CMOS Integrated Resistors

There are a number of integrated precision resistor options available to IC designers on various silicon processes. Poly-silicon resistors currently and historically are the most common resistor type in standard complementary metal–oxide–semiconductor (CMOS) processes due to use of standard materials. Further improvements on poly-silicon resistors in terms of matching, linearity, noise and temperature dependence were achieved with Tantalum Nitride (TaN) resistors. TaN resistors were developed in the 1980’s for the analogue semiconductor industry. Technology advancements on TaN resistors were accomplished with the introduction of SiCr and NiCr resistors for analogue ICs. High precision SiCr resistors were the first adopted by Analog Devices in the early 1990’s [43]. Companies such as Texas Instruments, who were initially using NiCr, switched to SiCr due to NiCr resistors’ sensitivity to mechanical stress which initiated drift in absolute resistance value during assembly [38]. SiCr is currently the dominant integrated resistor technology for silicon CMOS processes and is currently used by the main analogue semiconductor companies Analog Devices, Texas Instruments and STMicroelectronics [44].

- P+ doped poly-silicon resistors use the same poly-silicon as that used to form the high quality gate in MOSFET devices. Boron used in the doping of the source drain regions is used to dope the poly-silicon resistor P+. A rapid thermal anneal at temperatures greater than 1000 °C is then used to activate the doping. The thickness and doping levels determine the sheet resistance, TCR and VCR of the resistor. Low doping of the poly-silicon resistor will give higher sheet resistance values such as 1100 Ω/□ reported by Thewes [42]. High sheet resistance values though are reported to have high VCR values of -800 ppm/V and high TCR values...
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of -750 ppm/°C [36]. Pflanzi shows that to achieve a low TCR poly-silicon resistor, of value -56 ppm/°C, a negative TCR film poly-silicon needs to be placed in parallel with a positive TCR poly-silicon film. While this lowers the TCR, the VCR is still relatively high at -700 ppm/V and the sheet resistance decreases from 1200 Ω/□ to 650 Ω/□. Poly-silicon resistors are cheap to implement into the CMOS process as no extra masks are required and all material used is standard [37]. In Figure 1-5, a cross section of a poly-silicon resistor is shown with the pol-silicon comprised of the gate of a MOS device as seen from the field oxide located beneath the resistive film. The main disadvantage of a poly-silicon resistor is the poor matching due to grain size variation [42]. This has been reported as up to 10 % mismatch between resistors.

![Cross section of a poly-silicon resistor](image)

**Figure 1-5: Cross section of Silicon die with a poly-silicon resistor [45].**

- Tantalum Nitride resistors were favoured in the 1980s over SiCr and NiCr resistors as the tantalum material was naturally robust against humidity penetration of early passivation [46]. SiCr and NiCr were found to be easily oxidised without sufficient protection from moisture. As passivation coatings along with SiCr and NiCr film’s specification values improved, an industry move was made away from Tantalum. Tantalum is still used for producing discrete resistors in applications where there is high humidity exposure but are considered expensive compared to NiCr equivalents.
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- Nickel Chromium (NiCr) Resistors have relatively high resistance, good matching and low TCR. The main disadvantages of NiCr are the extra processing steps required to implement the film, the non-standard materials and the low sheet resistance. NiCr resistors are processed similar to SiCr resistors with the use of sputtering technology. It is obvious that NiCr TCR values from Table 1-1 and Table 1-2 are higher for an integrated resistor. This is because discrete resistors deposit NiCr on substrates with lower thermal coefficients of expansion than compared to the standard SiO₂ substrates of integrated solutions. The lower thermal coefficient of expansion limits the negative TCR and therefore reduces the absolute TCR value.

- Silicon Chromium has a higher sheet resistance compared to NiCr. SiCr is approximately 1000 Ω/□ compare to 200 Ω/□ for NiCr. This results in SiCr resistors having a smaller surface area for resistors requiring high resistances. SiCr resistors have good matching, low TCR of typically -25 ppm/°C, and relatively high current densities [47]. The PCR values of the integrated resistors are quite high due to the resistor being deposited between metal interconnect layers in the IC die rather than near the Silicon substrate. This results in a lot of self-heating if a large amount of power is dissipated. These resistors generally conduct low current densities and therefore avoid any significant variations due to the PCR. Like NiCr resistor processing, extra process steps are required for implementing the SiCr resistor on a CMOS process. SiCr is found to be a more stable compound compared to NiCr. This is seen after assembling the silicon die into package where absolute value in a NiCr resistor can have changed by several hundred parts per million while an equivalent SiCr resistor would have changed by a couple of hundred ppm or less [38].

It can be seen from Table 1-1 and Table 1-2 that the best available resistor technology are metal foil resistors. The dominant supplier of this type of resistor is Vishay which sells their resistors under the Bulk Metal Foil brand. These resistors cost up to $ 40 [29] making them one of the most expensive components on any PCB board and regularly more expensive than the IC to which it is connected. More commonly used external precision resistors are the 5 ppm/°C thin metal film resistors which provide
accuracy at an affordable price. Current integrated resistors match external resistors resistance tolerance value but not in terms of other performance criteria. In particular, temperature related specifications are significantly worse than external resistors. IC companies have tolerated the high TCR values by improving tracking between resistors. This is adequate in circuits such as circuit dividers and digital to analogue converters (DAC) R-2R ladders but not in current shunt applications. When an individual resistor is required the IC manufacturer needs to specify the external resistor required in the datasheet. This lack of low TCR integrated resistor technology increases cost for the customer, decreases reliability on the final PCB as there are more external components and reduces potential profits for the IC manufacturer.

1.3. Trimming Techniques

Trimming of resistive materials was developed to correct for processing variations that affected resistor properties. These subtle variations included uneven film thicknesses and rough periphery definition in the range of nano-meters. Even slight differences in anneal times or applied temperature in ovens with 1 °C tolerances can result in mismatch of film electrical properties. For standard resistors, these minor effects would be insignificant but for precision resistors measured in terms of ppm the effects are found to be considerable. To date, only LASER trimming has been successfully commercialised to achieve resistors with extremely accurate absolute values.

1.3.1 Bulk Material LASER Trim

LASER Trim is used to accurately trim a resistor to a desired absolute value. LASER trimming is commercially used for trimming poly-silicon, SiCr and NiCr resistors. LASER trimming operates by vaporizing part of the film and therefore increasing the resistance of the film [48] [49]. Initially, it was found that trimming the main body of the resistor created areas of stress on the film due to the high temperatures experienced during the trim [50]. These areas of high stress resulted in an increase in noise for the resistor. Through the use of LASER trim tabs on the sides of the film, these stress areas were moved away from the main current path and avoided an increase of
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noise. LASER trimming has been commercially used for more 20 years and is regarded as a highly reliable trimming process. Disadvantages of LASER trimming include the necessity for special equipment for the process of trimming and that the trim must be carried out prior to assembly of the die into the package.

Figure 1-6: LASER trimming of a resistor. Image taken from www.ami.ac.uk [51].

1.3.2 LASER Fuse Trim

Fuses can be used to accurately trim a resistor. As seen in Figure 1-7, if the material is seen to have a constant sheet resistance, the trimming of the large link or fuse will result in an increase in resistance.

Figure 1-7: Image of Vishay Z-foil audio resistor, taken from hifiduino.wordpress.com [52], and a diagram of the links used to trim the absolute resistance taken from Vishay [33].
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A high energy LASER beam or a high current can be used to open circuit the fuse. A LASER may be used to blow fuses rather than directly trim the film if the main bulk films surface area is smaller than the LASER beams cross sectional diameter. The LASER trim requires a special tester and can only be carried out prior to assembly. The advantage of the electrical blowing of the fuse is that the trim can take place post assembly. The disadvantage for the current trim is that large die area needs to be dedicated for the circuitry to control and supply the high currents required for the trim. The main disadvantage of using fuses for trim is that it may not be as precise as the bulk LASER trim. This is because the accuracy of the trim is dictated by the number of fuses available.

1.3.3 Thermal Anneal Trim

A thermal anneal trim applies a thermal bias to the film to induce a material change. This material change can alter the absolute value resistance and the TCR of the film. A number of methods have been implemented for the thermal bias. One of the initial thermal trimming methods was through the use of low power LASER annealing of the film [50]. This anneal resulted in high stress areas on the film as found with bulk LASER trimming. These high stress areas affected the electrical noise parameters of the resistor. Another attempt was made by applying a high current across a poly-silicon resistor to induce self-heating. This method was successful but large currents, 10 mA/µm², were required for the trim [53]. Microbridge Technologies [54] is the more successful of the thermal anneal trim methods as the required current was reduced by etching a trench below the resistor to thermally isolate the resistor from the silicon substrate. Figure 1-8 shows a section of the Rejustor resistor with the poly-silicon resistor wrapped around a heater element. The heater element is used to anneal the poly-silicon resistor. This method requires a large area for the resistor and a special process to etch below the resistor. Even with these extra processing steps, the trim applied to a poly-silicon resistor can only achieve at best a TCR of +/- 100 ppm/°C which is much higher than standard deposited films. Further attempts included a heating element below the resistor to change the films properties [55]. This method requires a large area and extra circuitry for the heating element.
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1.4. \textit{iTrim} Method

From analysis of current resistor technology, there is a clear requirement for a near ideal resistor that can be integrated together with an IC. To date, no technology has been successful in meeting the standards required for commercial release. The \textit{iTrim} method has been developed as a trimming method that not only corrects absolute resistance value but also other specifications such as TCR, PCR and VCR. The \textit{iTrim} method uses automatic tester technology found commonly in the IC industry to correct for process flaws produced by the most advanced fabrication equipment. The \textit{iTrim} method was discovered during a study into the reliability of SiCr Thin Film Resistors. The aim of this study was to increase current density limits used by designers when specifying SiCr resistors for an IC. The standard current density limits were proportionally lower than other common resistive films such as poly-silicon. This resulted in a wider SiCr resistor than was necessary if the standard limits were proven to be too conservative. It was desirable to increase the current density rules while still retaining the stable properties of

Figure 1-8: Optical image of a Rejustor resistor.
the SiCr film. To increase current density limits the failure of the TFR needed to be understood and modelled.

Previous publications [56] [57] have discussed the failure mechanisms found to date. The failure modes consist of a decrease in resistance followed by a fusing event when stressed with a constant bias. Standard reliability testing of SiCr comprises of stressing a TFR with a high current density in extreme ambient temperatures, typically greater than 200 °C. In Figure 1-9, a plot shows the change in resistance over time as a resistor is stressed in these extreme conditions. This is a typical result when a resistor is overstressed resulting in an initial drop in resistance followed by a fusing event and open circuit. The SiCr test structures comprise of a 4-wire Kelvin arrangement using the metal interconnect above the resistor. The resistor itself is surrounded by oxide and is placed between interconnect metals two and three in the IC stack. Due to the high current densities and the surrounding oxide limiting thermal dissipation, resistor junction temperatures during the stress can exceed 500 °C. It is this high temperature that results in the material change within the SiCr resistor. This material change starts in the centre of the resistor as this is the hottest point as seen in Figure 1-10.
Wafer level stressing was carried out in ambient temperatures to understand the failure mode found during the stress tests. The wafer level test consisted of three forward and reversed power sweeps applied across a resistor. Each forward power sweep stopped at a defined max power and was then followed by a reverse ramp back to 0 W. The maximum power points were chosen to allow for a permanent drop in absolute resistance. In Figure 1-11 the temperature of the film is measured for the initial forward sweep and the final reverse sweep. The temperature from the forward sweep, solid blue line was found to be higher than with the equivalent power density in the reverse sweep, dashed blue line. It was discovered that when the film gains enough energy the Silicon Chromium compound, SiCr, adapts itself by splitting off silicon atoms and forming a more metallic compound. This change occurs in the centre of a standard SiCr film and reduces the resistance resulting in a lower power density for the reverse sweep. This lower power density results in a lower junction temperature for the film during the reverse sweep compared to the forward sweep. The iTrim method is based on this permanent decrease in resistance generated by stressing the film with a high current density. Not only does the absolute resistance change but the entire thermal and electrical properties of the film become more metallic. This results in an increase in TCR as the absolute
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resistance decreases. Repeated short stresses of the film with high current densities can control how much the film is changed as seen by the repeated power sweeps in Figure 1-11. To determine when the resistor has been optimized, the slope of the power versus resistance relationship or PCR of the resistors can be used as a reference.

![Initial forward sweep and Final reverse sweep](image)

**Figure 1-11: Wafer level power sweep of a SiCr resistor.**

Once the slope is flat or PCR equals zero, it can be assumed that the TCR of the resistor is near or at a value of 0 ppm/°C. This is due to the dependence that the PCR value has on the average TCR of the film. The use of the PCR as the reference for TCR allows for the possibility of single temperature testing and trim of the SiCr resistor. *iTrim* is a novel method discovered, evaluated and developed from the work presented in this thesis. The trimming method allows for the advancement in the precision of IC technology by allowing designers to work with near ideal performing resistors. This thesis will demonstrate the trimming of both the absolute resistance and TCR to predetermined values while restricting the test and trim to a single ambient temperature. This combination allows for commercially viable trim of an integrated resistor that competes with the high precision external resistors.
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1.5. Discussion and Thesis Overview

The aim of this thesis is to demonstrate the trim of a SiCr resistor’s absolute resistance and TCR to set predetermined values. The thesis will continue in Chapter 2 with a more detailed background on SiCr resistors and the conduction mechanisms that combine to give the resistor its excellent thermal and electrical properties. Chapter 3 will present data on the electrical and thermal properties of the resistor. A detailed explanation will be given on the use of the PCR of the resistor to predict the TCR of the film. This predication of TCR using a single electrical test at room ambient conditions is key in making \textit{iTrim} a successful trim method. Chapter 4 will present the method behind the electrical trim and detail, using TEM images, the changes that occur in the SiCr film during a trim cycle. A SiCr resistor model will then be presented that is used in Analog Devices proprietary circuit simulator, ADICE, that allows for the accurate simulation of a PCR measurement and the electrical trimming method. This model is based on earlier data from Chapter 3 and 4. Chapter 4 will conclude with a design review of a 10 kΩ resistor designed to have its absolute resistance and TCR trimmed to predetermined values using the \textit{iTrim} method. Chapter 5 will present data from the X452B test chip which contains the 10 kΩ \textit{iTrim} cell. Data will demonstrate the successful trim of the 10 kΩ resistor. A reliability analysis will then show the results of samples of the post trim test chip after various electrical, thermal and mechanical acceleration tests. These tests will demonstrate the robustness of the post trim resistor. Chapter 6 will conclude the thesis reviewing the previous data that supports the use of the \textit{iTrim} method on a commercial product. Future work will detail how the trim method can be improved further to achieve greater accuracy and stability.
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1.6. Bibliography


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Chapter 2: Silicon Chromium Processing and Theory

2. Silicon Chromium Processing and Theory

Silicon Chromium thin films have been incorporated by the semiconductor industry into integrated circuits to provide stable and reliable resistors for over twenty years. Although available for twenty years, only the leading analogue IC vendors were capable of using these resistors in their precision IC devices. This was due to the requirement of significant investment to support internally owned fabrication plants that developed analogue specific processes. Recent analogue processes provided by foundries such as Dongbu’s HP180 process [1] are listing Silicon Chromium resistors as an option for their processes allowing the entire analogue IC industry access to these precision components. The overall construction of Silicon Chromium resistors from various internal and foundry processes are similar in terms of layout [2] [3] [4] but performance differences can be put down to variations in process recipes. Process recipes being the dopant levels, power, time and temperatures required for each step, such as deposition, anneal, lithography and etch, of the fabrication process. For the remainder of the Chapter, the Silicon Chromium resistors will be referred to as SiCr due to the variations in film doping and processing. In the following Chapter an overview of Analog Devices SiCr resistors will be provided and the integration of the resistor into the various processes and geometry nodes ranging from 2 μm to 0.18 μm will be explained. An overview of processing and post processing will be provided along with explanations on how subtle differences in recipes produce variations in the electrical and thermal properties that affect the performance of the final SiCr film.
2.1. ADI Thin Film Resistors

Analog Devices develop internal fabrication processes in order to meet the requirements of various precision IC components. Current digital IC manufacturers are producing state of the art logic IC devices at the 14 nm node to take advantage of the speed and transistor density at these geometries. Analog circuit manufacturers on the other hand are still making state of the art precision ICs at the 2 µm nodes. This is because ICs such as instrumentation amplifiers require bipolar transistors, which are quite large relative to digital CMOS logic, in order to reduce noise and therefore increase precision. ICs such as precision DACs are currently manufactured using 0.35 µm BCDMOS (Bipolar, CMOS and DMOS) technology with current development at the 180 nm node. For these components, there is also a requirement for higher density in order to reduce cost. In the majority of Analog Devices’ internal processes, SiCr resistors are provided as a process option. The advantage of the SiCr resistor over other options such as poly-silicon resistors is the excellent matching and low TCR. Products such as the AD5791 have specifications such as linearity and drift performance, which rely on the performance of the SiCr resistor.

2.1.1. ADI Thin Film Resistor Structure

One of the first publications for ADI’s Thin Film resistor was in an ADI patent granted in 1991 [5]. An example of the final resistor can be seen in Figure 2-1. When comparing the resistor presented in the original patent and that as seen in Figure 2-1, it is realised that the basic construction of the resistor has remained the same for over 20 years. Improvements have been made in lithography and process controls, which reduce the minimum dimensions of the resistor and improve the periphery definition. The position of the resistor in the process stack has also changed from originally being placed directly on the Silicon substrate to moving the resistor higher in the stack. The advantage of positioning the SiCr resistors between metals is the possibility of locating other circuitry below the resistor which is not possible with poly-silicon resistors. The resistor itself is comprised of a 1000 Ohm per square (Ω/□) SiCr Film. The SiCr is sputtered onto a bed of Silicon Dioxide (SiO₂). A Titanium Tungsten (TiW) layer is then deposited on top of the SiCr film to act as contacts. Tungsten vias join the TiW contacts to the
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Aluminum Copper (AlCu) metal through the inter layer dielectric (ILD), comprised of SiO₂, located above the SiCr film.

![Figure 2-1: ANSYS model of SiCr Resistor layout.](image)

### 2.2. ADI Processes with SiCr Resistor Option

During the investigation in to *iTrim*, a number of test ICs were produced on various processes with SiCr resistors. These processes include a 0.35 µm process and a 0.18 µm process. The construction of the resistor remained the same but the position of the resistor in the back-end stack varied depending on the process used. Figure 2-2 shows a cross section of ADIs 0.35 µm process. In the 0.35 µm stack the resistor is positioned beneath the third metal layer. The disadvantage with having the resistor so low in the stack is the restriction of not having enough metal layers to allow for overlapping of interconnects underneath the resistor to connect devices. In order to allow for greater device density, the SiCr resistor was moved beneath metal five in the 0.18 µm process. As shown in Figure 2-3. This allows for devices such as transistors and capacitors to be positioned beneath the resistor therefore reducing required silicon surface area.
SiCr is found to be a very durable material. Therefore a large power density can be reliably dissipated by the resistor during operation. The disadvantage with moving the resistor higher in the IC stack is that there is more SiO$_2$ between the resistor and the bulk silicon substrate, which acts as a thermal heat-sink for the dissipated power. SiO$_2$ is found not only to be a good electrical insulator, but also an excellent thermal insulator. Therefore, for a given power density, the junction temperature of the resistor will increase.
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as it is positioned higher in the IC stack. This has adverse effects on the self-heating and power rating for the resistor.

2.3. Silicon Chromium Film Processing and Structure

ADI uses a SiCr film comprised mainly of Silicon and Chromium mixed with various dopants to create a film with sheet resistance of 1000 $\Omega/\square$ and a TCR of around -25 ppm/$^\circ$C. A basic outline of ADI’s process in producing the SiCr film consists of sputtering the cermet material onto a SiO$_2$ layer and then annealing the film at a defined temperature for a given period. To generate a low TCR and high resistance from this process, many factors need to be adjusted. These factors include SiCr composite ratio, deposition method plus anneal temperature and time. When these factors are defined, they are combined to form a process recipe for that film.

2.3.1. Silicon Chromium Deposition

The main methods used to deposit SiCr films include physical vapor deposition sputtering (PVD) [3] [6] [7] [8] [9] [10] [11] and high density plasma chemical vapor deposition [12]. Based on the number of papers produced related to SiCr resistors, the assumption can be made that PVD sputtering is the dominant method used in industry with Texas Instruments [3], Vishay [13] and Philips [5] all reporting to use the method. The PVD process takes place in an ultra-high pressure chamber. A typical sputtering process starts by creating a high pressure vacuum of less than one ten millionth of an atmosphere. An inert gas, usually Argon, is then introduced to the chamber. The inert gas contains a majority of neutral atoms and a minority of positively charged ions. These ions accelerate towards the negatively biased SiCr target. Some ions collide with inert gas atoms creating more ions and free electrons while others hit the target and displace Chromium and Silicon atoms if there is sufficient energy. The magnet located behind the SiCr target holds the ions close to the target creating plasma. The plasma maintains the process of creating new ions which continue the displacement of additional atoms from the target. The displaced high energy Silicon and Chromium atoms move towards the
grounded substrate exchanging energy through collisions. The Si and Cr atoms continue to collide with other atoms until they successfully bind to the substrate or are reabsorbed by the target. As more atoms are bound to the substrate, a thin film is formed. The longer the sputtering process, the thicker the film. Figure 2-4 shows an example of a PVD sputtering system.

Figure 2-4: PVD Sputtering system.

The process of Silicon and Chromium atoms binding to the substrate is referred to as nucleation with the initial atoms to successfully bind to the substrate being called the nuclei. Islands form around these nuclei as more atoms bond to the substrate. If there is a strong similarity between the deposited atoms to the substrate material the nucleation density is strong, forming large two dimensional monolayer islands. As these large islands continue to grow, the islands collate covering the substrate with a continuous film. This growth mode is called Frank-Van der Merwe mode [14], as seen in Figure 2-5 A, and is the growth mode for the Silicon atoms deposited onto the SiO₂ substrate. Unlike the strong affinity between Silicon and SiO₂, Chromium islands tend to follow the Wolmer-Weber growth mode [14], as seen in Figure 2-5 B, where islands tend to grow in a way that reduces the interaction between the metal atoms and oxide substrate.
Figure 2-5: Frank-Van der Merwe growth (A) and Wolmer-Weber growth (B).

If there is sufficient Chromium deposited, a continuous Chromium film will form on top of the Silicon film as seen in Figure 2-6 A. If the density of Chromium is insufficient for Chromium islands to collate, a discontinuous film consisting of Chromium sphere shaped islands within a Silicon matrix is formed as found in Figure 2-6 B. The diameter of the islands is limited by the thickness of the film. Therefore, thick films result in large
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islands with small distances between islands. With a post processing thickness of singular nano-meters the Analog Devices SiCr film will consist of many small Chromium islands with large distances between each island. As the SiCr film is discontinuous, an electron would find a high resistance path of MΩ value through the conduction band of the Silicon located between the Chromium islands. However the sheet resistance is found to have a relatively low resistivity of 1000 Ω/□. This is because carrier conduction is dominated by tunneling mechanisms in discontinuous films rather than the standard electron transport through the conduction band that occurs in bulk metals [15]. It is found that the size of the islands and the distance between islands has a significant effect on the electrical properties of the film. This is due to the change in domination between one conduction mechanism and a different conduction mechanism.

2.4. Silicon Chromium Conduction Mechanisms

The SiCr film used in this thesis is mainly comprised of Silicon and Chromium but there are dopants added to tweak the performance of the film. At the time of writing the dopants were unknown to the author due to the recipe being an internal Analog Devices trade secret. For the remainder of the thesis, the detailed knowledge of the dopants is not required but it can be presumed that the Silicon is doped and would have semiconductor properties. The metal island and silicon can be viewed as a metal-semiconductor contact. The potential energy diagram of a metal-silicon junction can be found in Figure 2-7.

In Figure 2-7, the Silicon has been n-type doped for this example. If this junction is forward biased with the metal island tied to a supply and the silicon tied to ground, electrons will flow through the conduction band of the Silicon into the metal island. The conduction methods used by these electrons to cross from the Silicon conduction band to the metal islands conduction band would be Schottky field emission, thermionic emission (TE), field emission (FE) and thermionic field emission (TFE) [16]. If the junction was placed in reverse bias, an increased sized depletion region will form between the metal and silicon which would repel any electrons attempting to mount the barrier. The only current flowing would be the result of field emission as electrons tunnel through the barrier. To avoid the rectification of a signal and the nonlinearity of the resistance in the
final resistor, there is a need to decrease the proportion of current flowing due to Schottky field emission and increase the probability of tunneling carriers being able to cross the potential barrier. To do this, the potential barrier width needs to be reduced. The first method to reduce the barrier is to increase the doping of the Silicon which narrows the width of the barrier [16]. The second method is based on the overlapping of image forces. If, in Figure 2-8, there is a negative charge located between the two metal islands with minimal separation distance, less than 10 nm, there will be an electrical image of this charge in both metal islands. The overlapping of these image forces results in a drop of the potential barrier [17].

**Figure 2-7: Potential barrier for metal-silicon junction [16].**

Figure 2-8 shows two metal islands located less than 10 nm from each other. Where Ef is the metal Fermi level and Ec is the bottom edge of the conduction band. The minimum distance and the extra doping reduce the original dashed line potential barrier to the new solid line. The two metal silicon junctions are now effectively low ohmic contacts. This means that electron conduction related to Schottky field emission is minimal and can be ignored. The conduction mechanisms of interest left are thermionic emission (TE), field emission (FE) and thermionic field emission (TFE).
In literature, conduction related to field emissions or tunneling is found to be the dominant method for electrons in a discontinuous film to cross the potential barrier [10] [18] [19] [20]. When a potential bias is applied across the junction, tunneling allows carriers to pass through the potential barrier even though the energy of the carrier is less than the height of the potential barrier. The quantum tunneling resistance ($R_{FE}$) is defined by Equation 2-1 [19].

$$R_{FE} = \frac{h^2 L}{e^2 (2m \Phi)^{1/2}} \exp \left( \frac{4\pi L}{h} \left( \frac{2m \Phi}{h} \right)^{1/2} \right)$$

In Equation 2-1, $e$ is the electron charge, $m$ is the electron mass, $h$ is Planck’s constant, $\Phi$ is the potential barrier height, $L$ is the distance between islands, $r$ is the radius of the island and $d$ is the thickness of the film. Equation 2-1 assumes that there is a low potential applied between the metal islands which results in the resistance of the junction being independent of the applied field [18]. Conduction by thermionic emission involves the carrier passing over the potential barrier as indicated by TE in Figure 2-8. The lower barrier makes it easier for electrons to pass over the barrier when the electrons have gained sufficient thermal energy. Equation 2-2 describes the relationship between resistance related to thermal emissions versus effective work and junction temperature [17]. In Equation 2-2, $A_1$ is a factor dependent weakly on temperature and distance.
between islands, $\psi_0$ is the work function of the metal, $B$ is a constant, $k$ is Boltzmann's constant and $T$ is the junction temperature in Kelvin. When the resistance is differentiated with respect to temperature, a negative temperature coefficient is found in Equation 2-3.

$$R_{TE} = A_1 \cdot \exp \left( \frac{\psi_0 - Be^2}{kT} \right) \quad 2-2$$

$$\frac{d \ln R_{TE}}{dT} = - \frac{\left( \psi_0 - \frac{Be^2}{L} \right)}{kT^2} \quad 2-3$$

Electrons transferred through thermionic field emissions or thermally accelerated tunneling transfer through the barrier at a higher energy than electrons that transfer by field emission. This is because electrons that gain sufficient thermal energy start to ascend the potential barrier. As the electrons gain energy the barrier thickness reduces resulting in a greater possibility for the electrons to tunnel through the barrier rather than having to continue to gain energy to transfer over the top of the barrier by TE. The equation that describes TFE can be found in Equation 2-4 [15], where $C$ is a constant and $\kappa$ is the Silicon’s dielectric constant. In Equation 2-5, $R_{TFE}$ is differentiated with respect to the junction temperature. Similar to electron transmission by TE a negative temperature coefficient is found.

$$R_{TFE} = C \exp \left( \frac{e^2/kr}{kT} \right) \quad 2-4$$

$$\frac{d \ln R_{TFE}}{dT} = - \frac{\left( e^2/kr \right)}{kT^2} \quad 2-5$$

The final conduction method in the SiCr discontinuous film is related to standard electron conduction by valence electrons in the metal islands. The resistance of the metal
islands can be simply described by Equation 2-6, where $R_s$ is the sheet resistance of the metal and TCR is the temperature coefficient of the metal. The TCR of the metal island will be positive due to the increased scattering of the thermally energised electrons as temperature increases.

$$R_m = R_s \frac{r}{r_d} \left( 1 + \frac{TCR \cdot T}{1e6} \right) \quad 2-6$$

The four resistances, $R_{TE}$, $R_{FE}$, $R_{TFE}$ and $R_m$, can be modeled using Bieganski’s approach [19] as seen in Figure 2-9. It can be seen from the resistor model and the previous analysis of the individual conduction mechanisms that the processing of the SiCr film has a significant effect on the electrical performance of the final resistor. If it is initially considered that an extremely low ratio of Chromium is deposited relative to Silicon, the final film will result in tiny islands separated by large distances. In this scenario, the resistance of $R_m$ is irrelevant as the islands are so small. As there is a large distance between the islands, the potential barrier will be quite wide and electrons will find it difficult to tunnel through to another island. The principle conduction method would be for electrons, which achieve sufficient thermal energy, that they pass over the barrier by thermionic emission and conduct through the silicon to another island where another potential barrier will need to be surmounted. This obviously results in a very high sheet resistance for the SiCr film.

Figure 2-9: Simple resistor model of metal-silicon-metal junction [19].
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To reduce the sheet resistance, a number of factors can be altered in the SiCr film process recipe. These factors can be related to the ratio of insulator to metal in the film, the temperatures exposed to the film during processing and the thickness of the film. Felmetsger shows in Figure 2-10 the sensitivity of the electrical performance of the film to the thickness of the deposited film. This sensitivity is due to the limiting of island size by the thickness of the film. A strong correlation between sheet resistance and TCR is found.

![Figure 2-10: Sheet resistance and TCR (negative) as a function of the SiCr film thickness. Image from Felmetsger [8].](image)

As metal is deposited, any metal atoms in contact with the silicon substrate will have a higher energy than metal atoms that land on top of previously deposited metal atoms. The energy difference between the metal islands external atoms, those atoms that make contact with silicon, and the energy of the internal metal atoms is referred to as the surface free energy. Metal islands tend to grow in a way to reduce contact with the insulator substrate as proper bonding cannot occur, resulting in less tightly bound surface atoms at the metal insulator junction as indicated in Figure 2-5 B [17]. The temperature of the substrate and the temperature of anneal both contribute to the size and distribution of the islands. If, during, deposition the temperature of the substrate is higher the metal atoms will have sufficient energy resulting in greater mobility. This increases metal diffusion allowing for the metal to form into islands that have the lowest energy
configuration. The islands continue to grow by absorbing smaller islands located around them. This occurs as metal atoms require less energy to move from a smaller to a larger island than vice versa. During deposition, there will be a more random distribution of metal atom islands from bottom to top, as metal atoms at the bottom of the film have had more time to diffuse and form larger islands. The distribution of islands is found to be less variable if an anneal is carried out after deposition. This anneal allows for all metal atoms to have the same chance to gain a lower energy state.

Figure 2-11: Transmission electron microscopy images of (Cr$_x$Si$_{1-x}$)$_1$_$y$N$_y$ films with $C_{N2} = 0.5\%$: ( a ) $x = 0.2$, unannealed; ( b ) $x = 0.2$, annealed at 540ºC in N ambient for 1.5 h; ( c ) $x = 0.6$, unannealed; and ( d ) $x = 0.6$, annealed at 540ºC in N2 ambient for 1.5 h. Image from [20].

See Figure 2-11, copied from Fan Wu [20], for comparison of two different metals to insulator ratios annealed and un-annealed. The metal islands are the darker regions and
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silicon the light grey areas. With the same Chromium/Silicon mix of 60%/40%, Figure 2-11 D is compared to Figure 2-11 C to clearly see the effects of a post deposition anneal that produces larger islands. The lowest possible resistance is achieved if the metal islands have sufficient Chromium to merge and form a continuous sheet which would have a sheet resistance of less than 1 Ω/□. For the Analog Devices resistor, the sheet resistance requires a mix of conduction through metal islands and through silicon gaps to attain a sheet resistance of 1000 Ω/□. The requirement also for a low TCR of -25 ppm/°C means that the temperature coefficients of the various conduction mechanisms would need to balance without lowering the sheet resistance significantly.

Figure 2-12: Dependence of resistivity and TCR of Si\textsubscript{1-x} Cr\textsubscript{x} thin films on annealing temperature. Image from Gladun [21].

In Figure 2-12, Gladun [21] has experimented with various ratio mixes of Silicon and Chromium with a post anneal at different temperatures. The dependence of the post anneals film’s sheet resistance and TCR can be seen from this plot. The effect of annealing on the TCR of the SiCr film is found to be related to crystal growth within the film. Gladun reports that between 170 °C and 300 °C grains of CrSi\textsubscript{2} start to form within the amorphous matrix. These larger crystals have a more positive TCR, resulting in the
overall increase in TCR. The change in TCR with greater anneal temperature follows a percolation graph as presented in Figure 2-13. The critical percolation point is when the dominant conduction path changes from one dominated by tunneling to one which is dominated by conduction within the metal’s conduction band [17]. The 0 ppm/°C point should be located before the critical percolation point to allow for the fine balancing of the negative temperature coefficients related to $R_{TE}$ and $R_{TFE}$ plus the positive temperature coefficient related to scattering. As the amount of Chromium is reduced in the mix, further annealing can bring the TCR negative again as the limited chromium is rearranged to have a resistance based on more metal-silicon junctions than continuous metal paths.

![Figure 2-13: Absolute TCR versus critical percolation.](image)

The TCR values found in literature and presented in this thesis can be viewed as relevant to the temperature range that the TCR was measured in. As previously stated, the SiCr film at room temperature has a negative TCR based on the effect of thermionic emissions and thermally accelerated tunneling. Both of these methods are based on electrons gaining energy and progressing up the potential barrier. However at high temperatures the number of electrons available to energize will saturate. Simultaneously the scattering occurring in the metal islands will continue, resulting in a positive TCR. Once electron transfer by thermionic emission and tunneling has saturated, the positive TCR related to scattering will dominate and change the film to a positive TCR film as seen in Figure 2-14.
2.5. Electrical Trim of SiCr Thin Film Resistors

As introduced in Chapter 1, the iTrim method uses a current pulse to reduce the film’s absolute resistance and increase the thermal coefficient of resistance. This is not the first attempt at using a current pulse directly or indirectly to trim a SiCr resistor. The first published attempt was detailed in patent US 3603768 A [22]. In this patent, a high current pulse is applied to a SiCr resistor that is deposited onto a glass or ceramic substrate. There is no SiO$_2$ or passivation deposited on top of the SiCr resistor, so the film is left exposed to the surrounding environment. It was found that by trimming the resistor in an inert atmosphere, the resistance will decrease initially. If the electrical trim was performed in an oxidising atmosphere, the resistance would increase. By balancing these two methods various resistance values and TCR values could be reached. The change in resistance for a desired TCR value is calculated from a predetermined chart. Examples of the trim demonstrate an initial TCR of -460 ppm/°C being trimmed to a TCR of -68 ppm/°C and a resistance accuracy of 0.01 %. Other methods suggested to heat the resistor include the use of a hot probe, flow of hot gas or an integrated heater. Reliability results demonstrate a stability of 0.1 % post a 1000hrs life test. The limitation of this method is the precision of the TCR trim. To avoid relying on temperature testing the inventors use a look up chart which results in inaccuracies in the final TCR value, such that the minimum TCR demonstrated is -68 ppm/°C. The second published attempt of trimming a SiCr
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resistor was by Privitera in 2012 [23]. In Privitera’s paper, an integrated metal heater is used to heat the SiCr film. A resistance trim of up to 37 % of the initial value was demonstrated. The absolute tolerance of the trim is stated as between 1 % and 5 %. This method is solely aimed at trimming the SiCr resistors absolute resistance while sacrificing the initially low TCR. Post a 10 % trim, the TC will have increased to 50 ppm/°C. The high TCR may be acceptable in applications were a post trim accuracy of 1 % is desired. The restriction of this method is the accuracy. Also, in Privitera’s paper, the SiCr film seems to undergo a radical change in the heat treated areas. No reliability data is disclosed but it would be assumed that the stability of the resistor is affected by the trimming process. To improve on both methods it will be necessary to not only trim absolute resistance and TCR in a fully sealed package post assembly, but also to carry out the trim using a single temperature test. By reaching these goals, the iTrim trimming process will move closer to becoming commercially viable.

2.6. Discussion

In this chapter, a review was presented of the SiCr resistor used as the test device in this thesis. The construction and positioning of the resistor in the backend stack of the Analog Devices 0.18 µm and 0.35 µm were presented, highlighting the advantages of both processes. Using current and historic literature, an outline of the processing methods used in fabricating the SiCr resistor was given. The impact on processing the resistor was detailed while referring to current literature on how to improve the electrical properties of the SiCr resistor. It was found that the size and distance of islands in discontinuous films determine the conduction mechanisms and can result in a negative or positive TCR. A process can be tailored to allow for a required sheet resistance and TCR based on this knowledge. An overview was then given on the two previous attempts to trim a SiCr film electrically. Although both methods succeeded in trimming the absolute resistance and TCR, both are limited resulting in reduced commercially viability. It is believed that the iTrim method presented in the following chapters will move forward the technology towards reaching this commercial goal.
2.7. Bibliography


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3. Electrical and Thermal Characterisation of a Silicon Chromium Resistor

The previous two Chapters introduced the concept of an electrical trim method used to alter the electrical and thermal properties of a precision SiCr resistor. One of the novel aspects of the trim method is the simple and efficient characterisation of the TCR value at a single temperature. This characterisation is performed using the PCR of the resistor. In order to guarantee the accuracy of the TCR prediction with both the IC design simulator and the IC tester, a full understanding of the thermal mathematical models surrounding the PCR term is required.

In this Chapter, an initial overview will be given on the test structures used for the characterisation. This will be followed by a detailed explanation of the test system and its performance capabilities. The limits of the test system will restrict the accuracy of the model behind the prediction of the TCR value. Results from a series of tests on the fabricated resistor structure will then be evaluated using the test system. These data will be analysed to understand the relationships between the geometry of the resistor and the thermal plus electrical performance. From this assessment, the accuracy of the models will be derived. The predictability of the TCR is critical to the acceptance of the trim method as a commercial technique.
3.1. Experimental Structures

Experimental resistor structures were produced using an ADI 0.35 µm CMOS fabrication process with a backend stack that included SiCr resistors. The experimental structures consisted of SiCr resistors with varying widths and lengths. These resistors were laid out in an array to account for film variation across a wafer due to lithography, deposition, etch and stress effects. Therefore, test structures were always laid out with a dummy resistor either side to reduce random variation in electrical and thermal performance for a given structure. In Figure 3-1A, a simple schematic of two parallel arrays is shown. In each of the arrays only one resistor is connected to the pads. Each end of the resistor for test had two connections to individual pads with the positive Force and Sense pins common between arrays. This allowed for 4-wire Kelvin measurements which minimised any measurement error due to measurement setup, package bonding and metal interconnect connections to the resistor while restricting resistance measurement to the SiCr film between the tungsten vias either side of the resistor [1]. The Cadence Virtuoso layout [2] equivalent for the simple schematic can be found in Figure 3-1B. Figure 3-1C shows an optical image of the post fabrication test structure.

![Figure 3-1](image)

Figure 3-1 : A simple schematic of a Kelvin connected simple array structure with Cadence Virtuoso layout and an optical image equivalent.

A layout schematic of the various resistor test structures can be seen in Figure 3-2. The resistor test structures were grouped into two, twenty-four pad arrays called “quads”. Each quad had eight to ten different test structures. Each group is indicated by the dashed yellow line in Figure 3-2. All test resistors in a quad shared the same positive force and sense pads while having individual negative force and sense pads. The sharing of pads
minimised bonding in assembly, while the common quad structure allowed for easier assembly pin outs.

![Figure 3-2: Layout of multiple test structures with varying lengths and widths.](image)

The goal for the test structures was to understand the thermal and electrical properties of the SiCr resistor. The Silicon Dioxide insulator material surrounding the resistor has a large impact on the thermal properties. To evaluate the thermal properties of the resistor, separate wafers had a variation in the thickness of Silicon Dioxide between the resistor and the silicon substrate.

![Figure 3-3: Varying SiO₂ thickness.](image)

As seen in Figure 3-3 the two different inter layer dielectrics (ILDs) of Silicon Dioxide were grown to a thickness of 5.5 µm and 2.1 µm. These oxide thicknesses were equivalent to the oxide thickness beneath TFRs in the 0.18 µm and 0.35 µm process options respectively.
A 28 lead ceramic DIP package was used for the assembly of the test structures. This package is easy to handle, has a large pin count and can withstand extreme temperatures without mechanically stressing the test die. Eight resistors were bonded out per package. The pin-out of the package was standardised to allow for a fixed test setup. The standardised pin-out can be seen in Figure 3-4 where each neighbouring pair of matching colours represent the positive force and sense pins for individual resistors, while the neighbouring black and red pins represent the negative force and sense pins which are all connected together externally in the test setup.

**Figure 3-4: Standardised package pin-out.**

The particulars, such as length, width and pin-out, of the various resistor test structures can be found in Table 3-1 and Table 3-2 below. Also, details of the maximum voltage and current that can be applied to an individual resistor based on the voltage source of the test system are detailed in the next section. Only those resistors that could be stressed with a relatively high current density where bonded out to external pins.
### Chapter 3: Electrical and Thermal Characterisation of a Silicon Chromium Resistor

#### Table 3-1: Quad 1 resistor test structures pad configuration and pin-out

<table>
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<th>Structure</th>
<th>Resistor</th>
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<th>Length (µm)</th>
<th>Resistance (Ω)</th>
<th>Pins (S+)</th>
<th>Pins (S-)</th>
<th>Pins (F+)</th>
<th>Pins (F-)</th>
<th>Vmax (V)</th>
<th>Imax (mA)</th>
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### Table 3-2: Quad 2 resistor test structures pad configuration and pin-out

<table>
<thead>
<tr>
<th>Structure</th>
<th>Resistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
<th>Resistance (Ω)</th>
<th>Pins (S+)</th>
<th>Pins (S-)</th>
<th>Pins (F+)</th>
<th>Pins (F-)</th>
<th>Vmax (V)</th>
<th>Imax (mA)</th>
<th>Imax (mA/µm)</th>
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</table>
3.2. Measurement Test System

The test setup was required to perform a Kelvin resistance measurement of the test SiCr resistor under variable current loads and ambient temperatures. The setup consisted of variable supply and measurement system. The variable supply was capable of driving a stable and low noise voltage to a resistor. The measurement system needed to perform a relatively fast high precision measurement while also having low measurement drift with change in time and ambient temperature. An example plot of resistance versus differential voltage for a thin film resistor, using the test setup, is seen in Figure 3-5.

![Figure 3-5: Example voltage sweep on a thin film resistor.](image)

As can be seen from the plot in Figure 3-5, the resistor has a drop in resistance of 1600 ppm over the entire voltage sweep. To achieve reliable measurements the system would need to measure the resistance of this particular resistor to an accuracy of approximately 0.1 Ω or less than 10 ppm. The resolution of the voltage source needs to be 11 bits or 0.05%. These specifications, as outlined in Table 3-3, would have to be consistent across varying electrical loads and temperature.
Chapter 3: Electrical and Thermal Characterisation of a Silicon Chromium Resistor

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Voltage</td>
<td>20 V</td>
</tr>
<tr>
<td>Maximum Bias Current</td>
<td>20 mA</td>
</tr>
<tr>
<td>Minimum Bias Current</td>
<td>24 µA</td>
</tr>
<tr>
<td>Thermal drift in measurement</td>
<td>&lt; 1 ppm/°C</td>
</tr>
<tr>
<td>Resolution of Resistance</td>
<td>20 ppm</td>
</tr>
<tr>
<td>Forced Temperature Range</td>
<td>-40 °C -&gt; 125 °C</td>
</tr>
</tbody>
</table>

Table 3-3: Target Test system performance specifications.

The LTZ1000ACH [3] high accuracy reference was chosen as the base of the test setup voltage supply. The LTZ1000ACH has a low frequency noise contribution of 1.2 µVpp while delivering a reference voltage of nominally 7 V. As the required supply voltage is 20 V, the LTZ1000ACH reference is preferred over a lower voltage and lower noise reference. A lower voltage reference would require a higher gain to achieve the required output voltage which in turn would gain up the noise. This would result in an actual higher peak to peak noise than using the LTZ1000ACH. This reference also is extremely stable with a temperature drift specification of 0.05 ppm/°C and a long term stability of $2 \mu V/\sqrt{kHz}$. The rate of drift reduces over time hence the use of the square root of time($\sqrt{kHz}$) when defining drift. The drift of the voltage supply reference over time does not contribute to the measurement drift specification, as detailed in Table 3-3, rather this specification is dominated by the measurement system which is the 3458A digital voltage meter [4]. The 3458A also uses the LTZ1000ACH as the internal reference and it is here that the excellent stability specifications are important. The 3458A is based on a high accuracy multi-slope integrating ADC architecture [5]. The integration time for the measurement is based on the power mains frequency of 50 Hz which can be a significant noise source. The lowest suggested integration time selectable is a single power line cycle or 50 Hz; therefore this can be assumed to be the maximum bandwidth of noise in the measurement setup. A schematic of the LTZ1000ACH reference circuit can be seen in Figure 3-6. The important specifications to evaluate for this circuit are the output voltage and the low frequency noise.
Chapter 3: Electrical and Thermal Characterisation of a Silicon Chromium Resistor

Figure 3-6: Schematic of LTZ1000ACH thermally biased reference circuit.

The output voltage is simply the sum of $V_{be}$ voltage of NPN2, at point 1 which is typically 0.7 V, plus the Zener voltage which is specified as typically 7.2 V in an ambient of 25 °C and with a Zener current of 5 mA. This gives a typical output voltage of 7.9 V.

The noise for the LTC1000ACH is stated as wideband noise of $40 \sqrt{Hz}$. This noise is related to the output noise of the Zener diode indicated in Figure 3-6 by point 2. Other sources of noise at point 2 in the schematic can be considered negligible in comparison to the Zener noise.

In order to vary the supply, while introducing minimal noise, a digital to analogue converter (DAC) was required. The AD5791BRUZ 20 bit DAC evaluation board [6] was chosen as this DAC has a noise contribution of typically $7.5 \sqrt{Hz}$ as defined in the datasheet. The evaluation board also allowed for the addition of the LTZ1000ACH reference. The schematic for the AD5791 can be seen below in Figure 3-7 together with the reference buffer circuitry. The op-amp U3 amplifies the reference to provide the positive 10 V reference voltage while the op-amps U5 and U6 invert and gain the reference signal to provide the negative -10 V reference voltage. The AD5791 allows for 20 bit accuracy which is far greater than the 11 bit requirement. The low noise and high voltage bipolar operation of this DAC justifies its selection. All op-amps used in the
voltage source are AD8676 op-amps [7]. The AD8676 has high gain and more importantly low noise of 2.8 $nV/\sqrt{Hz}$.

![Figure 3-7: Schematic of the reference buffers and AD5791 DAC.](image)

The specification of interest for this circuit is the noise contribution. As previously stated the noise bandwidth of the 3458A is a maximum of 50 Hz. Therefore the noise within this 50 Hz bandwidth of the various components used is only considered. From the spectral noise density versus frequency plots in the datasheets of the AD5791 [6], LTZ1000ACH [3], AD8676 [7] and Vishay foil resistors [8], it can be seen that the $1/f$ noise contributes to typically 20 % of root mean square (RMS) noise while thermal noise contributes to 80 % of the RMS noise. Therefore, an approximation of the peak to peak noise in the measurement system can be relatively simply calculated by only considering the thermal noise of the various components. This approximation can be calculated by initially zeroing the noise on nodes 9 and 10 of Figure 3-7 as the 220 µF capacitors filter the generated noise related to the reference and op-amps. The noise on the Vout node can then be calculated using the thermal noise of the AD5791 and the noise sources from the output buffer. These noise sources being $I_{n_{amp}}$ and $V_{n_{amp}}$ which represent the current and voltage noise specifications of the AD8676 op-amp.
As can be seen from Equation 3-1, the total noise output from the buffer of the DAC can be calculated as 8.1 $nV/\sqrt{Hz}$.

To meet the maximum 20 V differential specification, an op-amp buffer network was created that directly buffered the DAC output to the Tungsten via of the SiCr resistor while also buffering an inverted signal to the opposite side Tungsten via. This meant that if the DAC was programmed to 10 V the result would be a 20 V differential applied across the resistor. The AD5791 evaluation board and op-amp buffer network were placed in an insulated container in order to minimise air turbulence induced low frequency noise [9]. The evaluation board can be seen in Figure 3-8.

Figure 3-8: AD5791BRUZ evaluation board with a LTZ1000ACH reference and Op-amp network [6].
As mentioned previously in this Chapter, the thin film resistor test structures were packaged in a 28 lead CERDIP with eight resistors per package. To minimise manual changes to the test system, when different resistors within the same package were required to be tested, a 34970A data acquisition switch unit [10] was used with two 34901A modules. The 34901A modules were capable of switching the voltage supply and measurement sense leads across a desired resistor for test. Figure 3-9 shows a simple schematic for the test system with two of the eight resistors connections for a particular device under test (DUT). As can be seen in the schematic, the force and sense lines can be
switched to a particular resistor using the force reed switches of 101 to 108 and the sense reed switches of 111 to 118. The first resistor’s force terminals are connected to switches 101 and the sense terminals to 111. The switches are ordered in an increasing sequence that means that 102 and 112 switches connect in the second resistor. This continues up to the eighth or last resistor which is connected to switches 108 and 118. In order to perform a Kelvin measurement, the 3458A meter would measure the voltage drop directly across the resistor under test and the voltage drop across a series shunt resistor labelled $R_{\text{shunt}}$ in Figure 3-9. A Vishay Z201 high precision and low TCR foil resistor [8] was chosen as the shunt resistor. From the voltage drop across the shunt resistor, the series current flow could be calculated. When the series current was divided into the voltage drop across the resistor under test, the resistance could be accurately calculated. In Figure 3-9, the 34901A modules are configured to measure the current flowing through the first resistor in the DUT as the switches 201 and 211 are closed and the switches 202 and 212 are open. In order to measure the voltage across the resistor in the DUT, switches 201 and 211 are opened and switches 202 and 212 are closed allowing for an efficient measurement time.

In order to determine the resolution of Kelvin measurement, the peak to peak noise of the voltage measurement was calculated. The approximate calculations for the noise error in the voltage measurements can be found below. It is assumed in the calculations that the resistor under test has a value of 10 kΩ. The resistor under test can have any value as listed in Table 3-1 and Table 3-2.

$$N_{13} = \sqrt{V_{\text{out}}^2 + V_{\text{amp}}^2} = \sqrt{8.1nV^2 + 2.8n^2} = 8.57 \frac{nV}{\sqrt{Hz}} \quad 3-2$$

$$N_{14} = \sqrt{\left( V_{\text{amp}}^2 * \left( \frac{R_{16}}{R_{15}} \right)^2 \right) + \left( \left( \sqrt{V_{\text{out}}^2 + 4kT(R_{15})} \right)^2 * \frac{R_{16}^2}{R_{15}^2} \right) + \left( 4kT(R_{16}) + ((R_{15} \parallel R_{16}) * I_{\text{amp}})^2 \right)}$$

$$= \sqrt{\left( 2.8n^2 * 1 \right) + \left( (\sqrt{8.1n^2 + 4.1n})^2 * 1 \right) + 4.1n + (500 * 0.3p)^2} = 9 \frac{nV}{\sqrt{Hz}} \quad 3-3$$
Ignoring lower frequency, higher magnitude spectral density 1/f noise, the root mean square noise at 50 Hz as:

\[ V_{\text{total}} = \sqrt{N13^2 + N15^2 + 4kT(R_{\text{shunt}}) + 4kT(R_{\text{DUT}})} \]
\[ = \sqrt{9nV^2 + 9.42nV^2 + 4.01n + 12.87n} = 13.7 \frac{nV}{\sqrt{Hz}} \]  

From Equation 3-7, the estimated contribution of thermal noise to the overall resolution specification would be 0.48 ppm for a 1 V drop across a resistor. The instrumentation noise is specified at 0.1 ppm at 50 Hz bandwidth [11]. Hence the noise from the supply dominates the measurement with minimal impact from the 3458A meter. In order to meet a 5 ppm specification a minimum measurement voltage of 0.1 V needs to be used. To achieve the accurate dc voltage measurement this would restrict the minimum bias current in the shunt resistor to no less than 0.1 mA. A minimum current of 0.1 mA is quite large given that the cross section of the SiCr resistor for test are so small and would result in significant self-heating. The self-heating would change the resistance and create an offset in the measurements. Therefore for precise measurements the integration time or number of power line cycles (NPLC) would be set to 1000. From Equation 3-9, the increase in integration time results in a 32x reduction in noise when compared to the peak to peak noise derived in Equation 3-7. This would mean the minimum current allowable during measurements would be approximately 3 µA in order to achieve a 5 ppm accuracy target. When less accurate measurements are required, the number of power line cycles would be reduced to achieve shorter test times.

\[ V_{\text{total}} @ 0.06Hz = 13.7 \times \sqrt{0.05} = 0.003 \text{ uVRMS} \]
\[ 0.003\text{ uVRMS} \times 5 = > 0.015 \mu Vpp \text{ to 99% CL} \]
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The required measurement drift and resolution specifications are based on the shunt resistor selection and the 3458A performance. The Z201 datasheet specifies a thermal drift of +/- 0.5 ppm/°C with a load life stability of 150 ppm over 10000 hours operation [8]. While the 3458A is specified with a thermal drift of 0.25 ppm/°C and a 24 hour drift of 2 ppm for the 1 V range [11]. If a laboratory temperature variation of 10 °C is assumed, a 7.5 ppm variation in measurements can be generated due to change in ambient temperature. As all precision measurements are completed in a 24 hour time period the drift, due to time, of both the Vishay resistor and the 3458A can be calculated as being a total of 2.5 ppm. This results in 10 ppm accuracy in the measurements due to drift. In total, the accuracy of the system would be 15 ppm when both noise and drift are considered.

To measure the temperature of the resistor under test, a DM314 PT100 platinum resistor temperature sensor [12] was used. A 34401A multi-meter [13] measured the resistance of the PT100 sensor, which was taped onto the package surface using thermally conductive Kapton tape. The temperature was calculated using the IEC 60751 temperature versus resistance tables [14]. To vary the ambient temperature of the package, a TP04310A airstream system (thermo-stream) [15] was used. The thermo-stream system is capable of changing ambient temperature in a range of -80 °C to 225 °C with a stability of approximately 1 °C. The temperature range was limited to between -50 °C, due to build-up of ice, and 150 °C, due to maximum safe use temperature of the socket. Figure 3-10 shows the laboratory setup used for the evaluation.
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Figure 3-10: Test setup.

The entire system, including voltage supply (AD5791), measurement system (3458A, 34970A) and temperature control system (34401A, TP04310A), were automated using Labview [16] software to allow for complex but repeatable measurements. Figure 3-11 shows a Labview screenshot incorporating a graph depicting resistance versus power for a resistor under test.
Figure 3-11: Labview screenshot of resistor measurement vi.
Table 3-4 shows the final specifications for the test system. The resistance measurement can be seen as a reliable measurement over a variety of conditions.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Voltage</td>
<td>20 V</td>
</tr>
<tr>
<td>Maximum Bias Current</td>
<td>20 mA</td>
</tr>
<tr>
<td>Minimum Bias Current</td>
<td>3 μA</td>
</tr>
<tr>
<td>Noise</td>
<td>0.5 μV_{p-p} (peak to peak) @ 50 Hz</td>
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<td>Thermal drift in measurement</td>
<td>0.75 ppm/°C</td>
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<td>Resolution of Resistance</td>
<td>15 ppm</td>
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<td>Forced Temperature Range</td>
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<tr>
<td>Temperature Tolerance</td>
<td>+/- 1 °C</td>
</tr>
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</table>

Table 3-4: Final Test System Performance Specifications.

3.3. Characterisation of post deposition SiCr resistors

The current trim method trims both the TCR and resistance to a predetermined value. As previously explained measuring the TCR in a product’s final test phase is time consuming due to the requirement to thermally sweep the resistor. To make the trim method cost and time efficient, the PCR measurement was used as a “meter-stick” or guide to predict the TCR value. The aim of the characterisation was to determine the accuracy of the TCR prediction using the PCR measurement.

The initial study took the simple four wire connected resistors discussed earlier in this chapter, and thermally swept them in order to extract the TCR. This resulted in the extrapolation of an equation which describes the connection between sheet resistance and
TCR. As discussed in Chapter 2, Section 2.4, this is based on the island structure of the post deposition SiCr material. The TCR measurement is comprised of performing a power sweep on the resistor at various ambient temperatures. From this power sweep, the PCR can be measured. An example of such a power sweep is seen in Figure 3-12 where the PCR can be taken as the 2\textsuperscript{nd} order coefficient of the polynomial fit, 5880.45 W/Ω, divided by the intercept resistance, 12524 Ω. This results in a PCR value of 469,534 ppm/W. The intercept point, 12524 Ω in Figure 3-12, is the resistance of the resistor with 0 W applied and is recorded as the resistance at the specific ambient temperature. An example of the intercept resistance versus ambient temperature measurement can be seen in Figure 3-13.

![Figure 3-12: Resistance versus Power for a 2 µm wide by 24 µm long TFR at 25 °C.](image)

The plot, in Figure 3-13, was generated by initially performing a power sweep at 25 °C. The temperature of the forced air, from the Thermo-stream, was dropped to -45 °C where another resistance measurement was made after a time delay to allow the device under test (DUT) to thermally saturate. The air temperature was increased in steps of...
10 °C up to 55 °C. At each step, after a thermal saturation delay, a power sweep was performed and the intercept resistance was extrapolated. Once the DUT completed the power sweep at 55 °C the air temperature was dropped back to 25 °C for a final resistance measurement.

Figure 3-13: Resistance versus Temperature for a 2 µm wide by 24 µm long SiCr resistor.

In total, the intercept resistance was measured three times at 25 °C. This confirmed that the sheet material had not changed due to the thermal ramp or power sweep and that the thermal saturation delay was long enough. If the maximum power, used in the power sweep, was too large for the resistor the electrical properties of the resistor would have changed. The higher the ambient temperature used in the TCR measurement, the lower the power requirement to make this change in properties. If the thermal saturation delay was not long enough, the three measurements at 25 °C would have shown a large variation. A compromise was required between saturation delay and an overall practical measurement time.
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From each resistor's plot of resistance versus temperature, a 2\textsuperscript{nd} order polynomial fit was applied. From the coefficients of the polynomial fit in Figure 3-13, the 1\textsuperscript{st} order temperature coefficient, Equation 3-10, and 2\textsuperscript{nd} order temperature coefficient, Equation 3-11, was calculated.

\[
TCR_1 = \frac{-0.218452}{12529.63} \times 10^6 = -17.43 \text{ ppm/°C} \quad 3-10
\]

\[
TCR_2 = \frac{0.000382}{12529.63} \times 10^6 = 0.03 \text{ ppm/°C} \quad 3-11
\]

As can be seen from the negative value of the first order coefficient, conduction within the SiCr film was dominated by tunnelling of electrons between islands. The conduction within the islands immersed in the SiCr film had an effect on the film resistivity, as seen with the existence of the second thermal coefficient. This second order coefficient was due to the resistance of the metal islands in the SiCr film having a positive temperature coefficient. Examples of the measured data for resistance, TCR and PCR for quad 1 and 2 arrays from wafers with two different stack heights, are found below in Table 3-5, Table 3-6, Table 3-7 and Table 3-8.

<table>
<thead>
<tr>
<th>Resistor Dimensions</th>
<th>Lot # D70408.3 wafer 6 Quad 1 (5.5 µm SiO(_2) thickness)</th>
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</thead>
<tbody>
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<td>W</td>
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</tr>
<tr>
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</table>

Table 3-5: Thermal and electrical measurement data for quad 1 resistor arrays deposited on 5.5 µm of SiO\(_2\).
### Table 3-6: Thermal and electrical measurement data for quad 2 resistor arrays deposited on 5.5 µm of SiO₂.

<table>
<thead>
<tr>
<th>Resistor Dimensions</th>
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</tr>
</thead>
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<tr>
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### Table 3-7: Thermal and electrical measurement data for quad 1 resistor arrays deposited on 2.1 µm of SiO₂.

<table>
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<th>Resistor Dimensions</th>
<th>Lot # D70408.3 wafer 7 Quad 1 (2.1 µm SiO₂ thickness)</th>
</tr>
</thead>
<tbody>
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<td>W</td>
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### Table 3-8: Thermal and electrical measurement data for quad 2 resistor arrays deposited on 2.1 µm of SiO₂.

<table>
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<th>Lot # D70408.3 wafer 7 Quad 2 (2.1 µm SiO₂ thickness)</th>
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</thead>
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</table>
3.3.1. Sheet resistance and TCR analysis

Altogether nearly 200 individual resistors were characterised over temperature. From these data, relationships between the geometry and sheet resistance of the resistors were discovered. Figure 3-14 and Figure 3-17 plot the sheet resistance (Rs), measured in Ohms per square (Ω/□), against the length and width of the resistor. The strongest link between resistors geometry and sheet resistance is seen with respect to the length of the resistor as plotted in Figure 3-14.

![Figure 3-14: Sheet resistance versus length of resistor.](image)

From Figure 3-14, it can be observed that there was a significant drop in sheet resistance the longer the resistor. This drop saturated with lengths greater than 40 µm. The percentage variation of shorter resistors can be extrapolated, if it is assumed that there was no variation in sheet resistance for neighbouring resistors on the same silicon substrate when resistors are greater than 40 µm in length. This extrapolation leads to a normalisation of the results which can be viewed in Figure 3-15. Using a power law fit, a reasonable prediction of the effect of length on sheet resistance was predicted. The cause
of this drop can be theorised as an over etch in the TiW contact which resulted in a thinner film at the ends of the resistor which gradually increased in thickness the further from the contact.

Figure 3-15: Systematic change in sheet resistance versus length of resistor, for neighbouring resistors.

As the over etch is an unexpected side effect of the TiW etch, the amount of SiCr film exposed to the etch is somewhat random. This results in shorter resistors not only having a systematic variation with length as seen in Figure 3-15, but also a random variation which gives rise to a larger spread the shorter the resistor. The extent of the spread can be predicted as seen in Figure 3-16, which also shows a good power fit.
Figure 3-16: Random variation in sheet resistance versus length of resistor, for neighbouring resistors.

From Figure 3-17, there seems to be no obvious width dependent variations on sheet resistance. As only a single quad was available per package it was not possible to get greater than two data points of variation in width for a given length per DUT. In future analysis it may be considered to do further quads that focus on width rather than length. This would provide a greater accuracy in the predicted sheet resistance for a given geometry.

Figure 3-17: Sheet resistance versus width of resistor.
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Figure 3-18 gives a simplistic view of the post etch SiCr resistor with an over etch at the TiW boundary which needed to be taken into account for any model of the electrical effects of a given resistor.

![View of a SiCr resistor with an over etch at the boundary with the TiW contact.](image)

**Figure 3-18: View of a SiCr resistor with a SiCr film over-etch at the boundary with the TiW contact.**

To evaluate the effect of ambient temperature on the resistor, the sheet resistance of the resistors were plotted with the corresponding measured first order thermal coefficient in Figure 3-19.

![1st order TCR versus Sheet Resistance.](image)

**Figure 3-19: 1st order TCR versus Sheet Resistance.**
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Figure 3-19 shows a linear relationship between sheet resistance and the 1st order temperature coefficient. The increase in sheet resistance indicates a thinner film which would have islands spread at greater distances from each other. This greater distance increases the dominance of electron tunnelling as the conduction mechanism within the film. The outliers from the linear fit are all at high sheet resistances and very low TCR values. These outlier data points are from measured resistors with a minimal length of 2 µm.

Figure 3-20 shows the relationship between the second order thermal coefficient of resistance and the sheet resistance. These data show that there is no specific relationship, but that the 2nd order TCR term is somewhat consistent for various data points. When these data are compiled into a histogram, as seen in Figure 3-21, data are centred at values of between 0.02 ppm/°C and 0.05 ppm/°C. The positive TCR term can be linked to the contribution of conduction through standard electron transport within the metal islands. This positive TC term will reduce with average island size. As in Figure 3-19, the outliers can be attributed to resistors with lengths of 2 µm. If resistors of length greater than 2 µm are used in a design, it is possible to predict the first order TCR term based on the sheet resistance and by taking a typical value, 0.03 ppm/°C, for the second order TCR term.

Figure 3-20: 2nd Order Temperature Coefficient of Resistance versus Sheet Resistance.
As described previously, for each resistor undergoing a TCR characterisation a PCR measurement was carried out at each temperature interval. The PCR is dependent on the thermal conductors surrounding the resistor dissipating the energy. For a resistor deposited directly onto the substrate, the dissipated energy would be easily absorbed by the high thermally conductive silicon substrate without significantly increasing the junction temperature of the resistor. The junction temperature will rise as the thickness of the oxide the resistor is deposited on increases. This is due to the reduced impact of the substrate in acting as a direct thermal conductor. Instead, the metal contacts and associated interconnect of the resistor start to dominate the thermal conductivity.

### 3.3.2. SiCr resistor Thermal Modelling

To be confident that the resistor has thermally saturated during a resistance measurement, there needs to be a delay greater than the thermal time constant of the surrounding SiO2. The delay required to thermally saturate the resistors junction temperature can be calculated based on the thermal time constant, τ, which is the time required to reach 63.2% of the final junction temperature. Equation 3-12 calculates τ to be 36.3 µs based on the thermal energy being dissipated from a surface area of 1 µm² and through an oxide thickness of 5.5 µm.
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\[ \tau = \frac{\rho \cdot c_p \cdot (A_s \cdot t_{ox})}{\left(\frac{G_{ox}}{t_{ox}}\right) \cdot A_s} = \frac{2.3e - 15 \cdot 730 \cdot (1 \cdot 5.5)}{(\frac{1.4e - 6}{5.5})} = 36.3 \, \mu s \] 3-12

Where:

\( \rho \) = Density (kg/\( \mu m^3 \))

\( c_p \) = Specific heat capacity (J/kg.K)

\( t_{ox} \) = Thickness of oxide between resistor and substrate (\( \mu m \))

\( G_{ox} \) = Thermal Conductivity (W.\( \mu m/K.\mu m^2 \))

\( A_s \) = Resistor Surface area (\( \mu m^2 \))

If the threshold for thermal saturation was assumed to be within 0.1% of the final temperature, the time to saturation can be calculated as being 250 \( \mu s \).

\[ -\tau \cdot \ln(0.001) = 250 \, \mu s \] 3-13

This calculation can be considered conservative as it only accounts for energy conducted directly down through the SiO\(_2\) and ignores the influence of thermal energy dissipating through the metal interconnect and around the resistor. What can be taken from this simple calculation is that the resistor will always be fully thermally saturated if a delay of greater than half a milli-second is included before a resistance measurement is taken. As Labview operates with a minimum delay of a single milli-second, the resistor can be presumed to be saturated when a measurement is required.

To appreciate the various effects of the thermal conductor, the collected data is studied to determine how thick the bed oxide, the resistor is deposited on, needs to be before the substrate loses its dominance in thermal conductivity. The temperature rise for a resistor with a length, \( L \), and width, \( W \), sitting on a bed oxide of thickness, \( t_{ox} \), and thermal conductivity, \( G_{ox} \), while dissipating a power, \( P \), can be calculated using Equation 3-14 [17].

\[ \Delta T = \frac{P \cdot t_{ox}}{G_{ox} \cdot L \cdot W} \] 3-14

This equation associates the thermal gradient from the resistors bottom surface to the area of substrate directly below the resistor of area \( L \) by \( W \). To get a model to fully
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represent the various thermal gradients the effect of the periphery area of the resistor and the distance of the contacts from the centre of the resistor needs to be taken into account [18] [19]. Equation 3-20 improves the accuracy of the calculated change in temperature compared to the actual change in temperature. It accomplishes this by first considering the thermal gradient associated with the resistor as an ellipse rather than a rectangle. Equations 3-15 and 3-16 use the length and width to calculate the radii associated with the ellipse. A value of 6 is added to the length of the resistor as the contacts have a length of 3 µm each and need to be accounted for in the surface area calculation.

\[ a = \frac{W}{2} \]  

(3-15)

\[ b = \frac{(L + 6)}{2} \]  

(3-16)

\[ h = \frac{(a - b)^2}{(a + b)^2} \]  

(3-17)

\[ t_{res} = 1000 \frac{L}{R_0 \cdot W} \]  

(3-18)

\[ \text{perimeter of ellipse} = \pi \cdot (a + b) \left( 1 + \frac{3h}{10 + \sqrt{4 - 3h}} \right) \]  

(3-19)

\[ \Delta T = \frac{P \cdot t_{ox}}{\left( G_{tha} \cdot (a \cdot b \cdot \pi) \cdot \frac{1}{t_{res}} \right) + \left( G_{thp} \cdot \text{perimeter} \right) + \left( G_{thc} \cdot W \cdot t_{res} \right)} \]  

(3-20)

Where:

- \( R_0 \) = Measured resistance of resistor
- \( t_{res} \) = Thickness ratio of SiCr film
- \( G_{tha} \) = Thermal Conductivity related to the resistor surface area.
- \( G_{thp} \) = Thermal Conductivity related to the resistor periphery.
- \( G_{thc} \) = Thermal Conductivity related to the distance from contacts.
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The variables $G_{tha}$, $G_{thp}$ and $G_{thc}$ are used as approximations of the thermal conductivity associated with the area, periphery and distance from the contacts. They are calculated by multiplying the actual thermal conductivity of SiO$_2$ by an individual constant which is based on the geometry of the resistor and the resistors position in the stack. Figure 3-22 demonstrates the thermal gradients associated with a resistor under bias.

$G_{tha}$ as stated above is based on the surface area of the ellipse based gradient shape. If the values for all the constants are extracted from measured data and $G_{tha}$ dominates the sum of the bottom line, in Equation 3-20, then it can be assume that the thermal energy is being conducted directly to the substrate below the resistor. This would mean that the horizontal thermal gradient between the resistor and substrate is steep and quickly drops off in temperature the further away from the resistor.

$G_{thp}$ is the constant that relates the thermal escape away from the periphery of the resistor. The perimeter of ellipse calculation in Equation 3-19 is a close approximation to the real value [20]. If the value of $G_{thp}$ is significant, this would indicate that the horizontal thermal gradients are quite large as the low specific heat capacity of the SiO$_2$ limits the vertical conduction of the thermal energy.

$G_{thc}$ is associated with the impact of the metal contacts and interconnect. As a resistor gets shorter there will be a greater impact of the metal thermal conductors on the average junction temperature of the resistor, Figure 3-23. The interconnect makes it easier for the thermal energy to conduct away from the resistor which spreads the thermal load to a wider surface area to travel down to the substrate which can be considered as the thermal ground. Like $G_{thp}$, the impact on thermal conduction of $G_{thc}$ will increase as the resistor is placed higher in the SiO$_2$ stack. In Equation 3-20, it is found that as the resistor gets wider and thicker, the thermal energy dissipates more readily through the contacts.
Figure 3-22: Impact of interconnect on thermal dissipation of resistor under bias.

To calculate the values of $G_{th_a}$, $G_{th_p}$ and $G_{th_c}$, a forced linear fit approach was used. Equation 3-21 was used together with the rearranged equation for TCR, Equation 3-22, to calculate the PCR value, Equation 3-23.
Various trial values were used together with the characterisation data of 200 resistors, including data from Table 3-5, Table 3-6, Table 3-7 and Table 3-8, in order to find the most accurate values for the three unknown thermal conductivity constants. The trial fitting process was based on the assumptions that resistors deposited close together would result in common constant values for $G_{tha}$, $G_{thp}$ and $G_{thc}$. A range of values were initially chosen for each of the three constants. The various combinations of these values were trialled using a program written for Analog Device’s proprietary circuit simulator called ADICE. Each trial produced a predicted PCR value for every resistor data point. The predicted values were plotted versus the measured values for PCR. A coefficient of determination of the straight line fit was then summed together with the value of the fit’s slope.
Figure 3-24: Fit data for various combinations in values for $G_{tha}$, $G_{thp}$ and $G_{thc}$.

Figure 3-24 depicts the fit results for predicted PCR data based on data from a set of eight resistors. The eight resistors were split into two groups based on the resistor’s width. During the fit process, the coefficient of determination, or fit, together with the slope was calculated for each group of four data points. If the predicted slope was less than zero, it was set equal to zero. The ideal trial, or count, occurred when both fits were close to a value of 1 and the slopes of both fits were close to 1. From the plot, trial 7214 was found to be closest to the measured data. Figure 3-25 shows the predicted versus measured data plot and the values from trial 7214. The stack height of 5.5 µm was considered a thick oxide between the resistor and the underlying silicon substrate. The constant value for thermal conductivity based on the periphery, $G_{thp}$, was greater than the area constant, $G_{tha}$, confirmed that the thermal gradients had a large horizontal spread. When the same analysis was carried out for an oxide of 2.1 µm, the best fit values were found to have a consistent $G_{tha}$ value with the 5.5 µm data while both the $G_{thp}$ and $G_{thc}$ decreased by 3x to 4x. This was because the resistor was closer to the substrate and therefore needs only to dissipate downwards using the resistor surface area available.
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Figure 3-25: Predicted versus measured values for trial 7214 with a $t_{ox}$ of 5.5 μm.

$G_{thn} = 0.8G_{ox}$, $G_{thp} = 1.8G_{ox}$, $G_{thc} = 8e^{-12}G_{ox} \times 1e^{12}$

Figure 3-26: Predicted versus measured values for trial 10080 with a $t_{ox}$ of 2.1 μm.

$G_{thn} = 0.8G_{ox}$, $G_{thp} = 0.65G_{ox}$, $G_{thc} = 2e^{-12}G_{ox} \times 1e^{12}$
3.3.3. SiCr resistor TCR prediction

In order to assess the accuracy of the extrapolated thermal conductivity constants, Equation 3-23 was rearranged to allow for the prediction of TCR based on the PCR measurements from all 200 resistors.

\[
TCR = PCR\left(\frac{G_{\text{thc}} \cdot (a \cdot b \cdot \pi)}{t_{\text{res}}} + \left(G_{\text{thp}} \cdot p\right) + \left(G_{\text{thc}} \cdot W \cdot t_{\text{res}}\right)\right) \tag{3-24}
\]

Figure 3-27 shows the cumulative frequency of errors in predicted TCR based on the extrapolated thermal conductivity constants and Equation 3-24. From this plot, it was found that there could be up to a 10 ppm/°C error in the calculation for TCR. When looking at the geometry of the resistors associated with the largest errors, it was found that the error was dominated from resistors with lengths of 2 µm and 80 µm. The errors in the 2 µm data were related to the random variation in the thickness of the film. While the errors in the 80 µm data were related to Equation 3-24 not taking the drop in thermal conductivity related to the contacts for long resistors accurately into account.

![Graph showing cumulative frequency of predicted TCR error versus measured error.](image)

**Figure 3-27:** Cumulative frequency of predicted TCR error versus measured error.
If data from resistors of length 2 µm and 80 µm are removed from the data set, the cumulative frequency plot in Figure 3-28 can be produced. Figure 3-28 shows a drop in predicted TC error to a maximum of 3 ppm/°C which is acceptable for a simulation.

![Cumulative frequency plot](image)

**Figure 3-28:** Cumulative frequency of predicted TCR error versus measured error with resistors of length 2 µm and 80 µm removed from data set.

The evaluation data for a given sized resistor can be used as guide for achieving a higher accuracy prediction of TCR value based on PCR measurement. As can be seen in Figure 3-29 the measured data confirms the linear fit between PCR and TCR as formulated in Equation 3-24.

![Linear fit plot](image)

**Figure 3-29:** Linear fit of TCR data versus PCR data.
If the linear fit is extrapolated from each set of resistors of equal geometry and a prediction of TCR is made based on this fit plus the measured PCR, an improvement should be found in the prediction. As seen in Figure 3-30 the error is up to 6 ppm/°C across all measured data.

![Cumulative frequency plot of error in prediction of TCR based on linear fit and PCR evaluation data.](image)

**Figure 3-30:** Cumulative frequency plot of error in prediction of TCR based on linear fit and PCR evaluation data.

If the data from resistors of length 2 µm is removed, the error in prediction can be further reduced. This is due to the random effects of the TiW over etch. As seen in Figure 3-31, the error is reduced to be nominally 1 ppm/°C.

![Cumulative frequency plot of error in prediction of TCR based on linear fit and PCR evaluation data less data with lengths of 2 µm.](image)

**Figure 3-31:** Cumulative frequency plot of error in prediction of TCR based on linear fit and PCR evaluation data less data with lengths of 2 µm.
3.4. Discussion

The goal of this chapter was to gather data to quantify the accuracy in predicting the TCR of a resistor using the measured PCR. This was accomplished by building an accurate and low drift test system that was capable of measuring TCR to ppm resolutions. From the data measured, two approaches to derive the TCR from the PCR were presented and explained. The first was based on an equation that uses approximate constants to describe the thermal behaviour of the resistor in the IC stack. This equation is targeted for use in an IC behavioural simulator such as ADICE. This model was found to be accurate to 3 ppm/°C for resistors longer than 2 µm which is acceptable for design. The second approach to TCR prediction was based on the linear relationship measured between PCR and TCR for a fixed resistor. This method resulted in an accuracy of 1 ppm/°C for resistors longer than 2 µm. This method would need to be characterised in an evaluation setup on the final product. The linear fit then would be programmed in the final test program to allow for greater accuracies during trim.

The next chapter will detail the characterisation of the trim on simple structures and the final model for the design simulator. A resistor will then be designed to allow for a successful integrated trim.
3.5. Bibliography


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Chapter 4: Electrical Trim; Background and Implementation

4. Electrical Trim; Background and Implementation

In this Chapter, a more detailed review of the trim methodology will be given together with a design review of the integrated circuit used to demonstrate the trim of the absolute resistance and TCR post assembly. The simple circuits in the previous chapter demonstrated the difficulty in predicting, to a high degree of accuracy, the TCR from single temperature electrical data. This chapter will open with a similar single temperature approach in predicting the change in TCR post trim. From these data, and that of Chapter 3, a model will be compiled to demonstrate the simulation of a thin film resistor in ADICE in a post fabrication configuration and a post trim configuration. The simulator will then allow for the design of a pair of integrated 10 kΩ resistors on a single die. Each resistor can be individually accessed for trim. The trim will be controlled using a Serial Peripheral interface (SPI) while two test points will allow for the electrical measurement of the 10 kΩ resistors. The end goal of this IC is to demonstrate that the absolute value and TCR can both be trimmed for an individual resistor.
4.1. Characterisation of Electrically Trimmed SiCr Resistors

To characterise the electrical trim of thin film SiCr resistors the same test setup is used as detailed in Chapter 3. The restrictions in the voltage and current limits of the supply rule out the use of Quad 2 structures for the trim evaluation. Therefore, Quad 1 structures results are reported. To characterise each resistor a short voltage pulse of around 10 ms is applied to the resistor. After each pulse a simple four wire resistance measurement is carried out or a full TCR characterisation is performed depending on the requirements of the test. Figure 4-1 shows the typical change in resistance for a given current flowing through the resistor. The change in resistance versus current sweep consists of three parts.

1. The first part is a small drop in resistance as current increases. This is a non-permanent change in resistance related to the self-heating and TCR of the SiCr film. This slope is defined by the PCR measurement.
2. The second part of the sweep is a rapid drop in resistance. This rapid drop is a permanent change in resistance and occurs, for this particular resistor, at an average junction temperatures above 300 °C.
3. The third part of the slope is a rapid increase in resistance. This increase is related to the mechanical breakdown of the SiCr film and once the bias is removed the resistors impedance will be typically in the range of 100 kΩ and above.

Figure 4-1 shows the current sweeps from a 2 µm x 10 µm resistor from wafer 7 and the same geometry resistor from wafer 6. Using Equation 3-20 from Chapter 3, a predicted average junction temperature can be derived. Figure 4-1 demonstrates that a larger current is required to achieve a permanent drop in resistance when the SiCr resistor is deposited closer to the substrate. This is logical as the resistor deposited closer to the substrate would have a greater thermal coupling to that substrate. It is also apparent that there is a smaller resistance drop for the resistor with a thicker bed oxide, before there is a mechanical breakdown of the film. Figure 4-2 shows two current sweeps for a 10 µm x 10 µm deposited on different oxide thicknesses. As seen in Figure 4-1, the resistor with the thinner oxide requires a higher current density to start permanently changing the film, but also has a larger drop in resistance before the film fuses. If the current density is
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derived, the wider 10 µm resistors require a lower current density, ~600 µA, compared to
the 2 µm resistors which require ~850 µA to reach the initial point of permanently
dropping the resistance.

Figure 4-1: Change in a 2 µm x 10 µm, 5 kΩ SiCr Resistor’s resistance due to higher
current stress and associated increase in junction temperature.

Figure 4-2: Change in a 10 µm x 10 µm, 1 kΩ SiCr Resistor’s resistance due to
higher current stress and associated increase in junction temperature.
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Figure 4-3 plots data from Figure 4-1 and Figure 4-2 with resistance change versus junction temperature. Considering the 2 µm wide resistors, it is apparent that the non-permanent drop in resistance versus temperature is the same. However when the resistance starts to permanently drop, the drop is at different rates depending on the stack thickness. This means that the reaction behind the change in the films properties is not only dependent on the average junction temperature but also the current density. The change in resistance related to the current density can at this stage be theorised as the electro-migration of silicon. If the Chromium was electro-migrating then the SiCr film’s resistance would increase. However as there is a greater decrease in resistance, it can be extrapolated that the silicon is electro-migrating and results in a higher ratio of Chromium to Silicon in the original material. This theory is further supported by data from the 10 µm wide resistors in Figure 4-3. Here, there is a greater drop in resistance from the resistor deposited on top of the thicker oxide. Also, this drop is not as significant as that found from the 2 µm wide resistors deposited on top of the same oxide thickness. This can be related to the lower current density required to trim a wider resistor and, therefore, the wider resistor has a lower rate of electro-migration.

![Figure 4-3: Resistance change versus junction temperature for a 2 µm x 10 µm and 10 µm x 10 µm resistors from wafers 6 and 7.](image-url)
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It can be concluded that the rate of drop in resistance is not consistent between resistors but heavily dependent on the resistor’s width, length and thickness of the underlying oxide.

4.2. Characterisation of current trimmed SiCr Resistors

If the test used to generate data in Figure 4-1 is repeated, collecting the absolute resistance value after each trim pulse as well as measuring the TCR value, changes in TCR with trim current can be viewed as in Figure 4-4. Figure 4-5 analyses the permanent resistance drop found in Figure 4-4 and produces a plot of TCR versus resistance.

![Figure 4-4: Plot of resistance change with trim current and TCR change with trim current. Resistor is 2 μm wide x 10 μm long from wafer 7 with 5.5 μm of SiO₂.](image-url)
In Figure 4-5, the resistors post fabrication resistance is 5308 Ω with a TCR of -19 ppm/°C. After the first trim pulse, using a defined voltage amplitude and pulse time, the resistance permanently drops to 5233 Ω and the TCR increases to -16.5 ppm/°C. If the trim was stopped at this point, the change in resistance and TCR would be permanent. The resistance should not return to the original pre trim value or reduce in resistance any further, as long as the current density used in the final application is minimal in ratio to the current density used for trim. The change in resistance and TCR in relation to a given trim pulse due to the electro-migration of Silicon can be modelled by Black’s equation [1] in Equation 4-1. The activation energy, defined by $E_a$, determines the amount of energy required for a thermal related reaction to occur. The current exponent, $n$, defines the acceleration component related to current density. In order to achieve a larger reaction or trim, a longer mean reaction time or a higher current density is required. The current density also governs the junction temperature if it is assumed all trimming occurs near
room temperature. The resistor is therefore trimmed further by applying a second pulse with increased voltage amplitude and/or a longer trim pulse duration.

\[
MRT = J^{-n}. \exp \left( \frac{-Ea}{k.T_j} \right)
\]

Where:

- MRT = Mean Reaction Time
- \(k\) = Boltzmann’s constant \((8.6173324 \times 10^{-5} \text{eV.K}^{-1})\)
- \(T_j\) = Junction temperature in Kelvin
- \(Ea\) = Activation Energy in eV
- \(J\) = Current density
- \(n\) = Current exponent

The rate of decrease in resistance in relation to increase in TCR, with trim, stays constant until around 0 ppm/°C. Once the critical percolation point has been passed, the slope of resistance change versus TCR change increases.

The TCR value is dependent on the specified temperature range. In Figure 4-6, the pre stress or pre trim condition shows a negative TCR below 300 °C while there is a positive TCR above 300 °C. The resistance bow is due to the limit in extra electrons available for conduction through tunnelling as temperature rises. After this point, the number of collisions between electrons, conducting within the metal Chromium islands, continues to increase with temperature resulting in a positive TCR. 300 °C is the point of critical percolation for the pre trim resistor. The \(iTrim\) method can be thought of as shifting this U-shaped curve until the point of critical percolation is at the trim ambient temperature which normally would be room temperature or 25 °C. This centres the low TCR to the usable temperature range.
A TCR value closest to 0 ppm/°C is likely to be the most desired value for applications requiring a high precision resistor with trim. To allow for an accurate trim without measuring the TCR, the PCR is used. Taking Equation 3-23 from Chapter 3, a relationship between PCR and TCR can be derived whereby the oxide thickness and thermal conductivity of the stack surrounding the resistor stay constant before and after trim. This relationship is seen in Equation 4-2.

\[
TCR = PCR \left( \frac{G_{th\alpha} \cdot \frac{(a.b.\pi)}{t_{res}} + (G_{thp}.p) + (G_{thc}.W.t_{res})}{t_{ox}} \right)
\]

\(y = 0.0004x^2 - 0.0155x + 0.1603\)

Critical Percolation Temperature = \(\frac{0.0155}{0.0004} = 39^\circ\text{C}\)

\[\Delta R \text{ (Ohms)}\]

\[\text{Temperature (DegC)}\]

\[\text{poly. (predicted post stress)}\]

\[\text{predicted pre stress}\]

\[\text{predicted post stress}\]

\[\text{TCR (ppm Ohms/°C)}\]

\[\text{Temperature (°C)}\]

Figure 4-6: Change in TCR with electrical trim for a 2.1 µm x 20 µm, 12kΩ Resistor.
Figure 4-7 plots data from three different resistors each from wafer 6 and wafer 7. The data are presented with TCR versus post trim measured PCR. A clear correlation is found between resistors from the same lots or with the same underlying oxide thickness. The slopes of the fit are equivalent to the value for thermal conductivity divided by oxide thickness, multiplied by 1 million. Data clearly show that the slope of the thinner, wafer 7, oxide resistors has a larger slope value and therefore a greater thermal conductivity and thinner oxide. The accuracy of the fit shows the use of the PCR value to track the TCR value during the trim is appropriate.

![Graph showing TCR versus PCR/Resistance for 10µm x 24µm resistors from wafer 6 (5.5 µm) and wafer 7 (2.1 µm).](image)

When trimming a resistor solely towards a specific TCR target, the method of using the PCR as the target is the best approach. If both the TCR and absolute resistance value are targets for the trim, then a method of predicting the change in TCR for a given change in resistance is important. However, as seen in Figure 4-8, even though the change in
resistance versus the change in TCR is somewhat predictable, it is not accurate enough to result in a precision trim.

\[ y = 6.523x^2 + 8.1988x + 5.5921 \]
\[ R^2 = 0.9976 \]

**Figure 4-8: ΔTCR versus Δ Resistance for a variety of resistors from wafers 6 and 7.**

In order to achieve a high accuracy trim, the resistor is split up into a number of equal valued and sized resistors linked in a string as found in Figure 4-9. One of the resistors can be chosen to perform a gross trim to a target value estimated based on an average fit of data in Figure 4-8. This target is initially approximately 150 % of the original TCR of that individual resistor. It will take a 300 % change to get the entire string to 0 ppm/°C. This initial gross trim can be used to calculate a more accurate fit for the change in TCR versus change in resistance. This fit should remain consistent between the resistors in the string if they are deposited close to each other, resulting in near exact thermal performance under trim. From the fit an extrapolation can be made to determine how much to continue the trim of the initial gross trim resistor and how much to trim the remaining two resistors. The addition of three resistance and TCR adjustments to the initial resistance and TCR values will result in the target values. This methodology will be discussed in greater detail later in this Chapter, when reviewing the design of the 10 kΩ test chip.
4.3. Failure analysis of a post-trim resistor

To understand what is occurring to the SiCr resistor during the trim process, a number of samples underwent transmission electron microscopy (TEM) analysis. This type of analysis was chosen due to the excellent resolution of the images produced. The first two samples were cross section samples or lamellae from an untrimmed resistor and from a trimmed resistor. Both lamellae were originally sourced from the same wafer and therefore had similar geometric properties. Figure 4-10 shows the cross section of the control or untrimmed resistor. When this is compared to Figure 4-11, a clear difference in the film thickness can be found. The trimmed resistor shows a thinner cross-section. Figure 4-12 shows the cross section view of the trimmed resistor at the TiW and SiCr film junction. In between the TiW and SiCr film a thin layer of Silicon can be found which is not present in an untrimmed resistor. The presence of this Silicon layer supports the electro-migration theory based on data in Figure 4-3 which shows a larger drop in resistance if a larger current density is used for the trim.
Figure 4-10: TEM cross sectional image of an untrimmed SiCr TFR.

Figure 4-11: TEM cross sectional image of SiCr TFR post trim.
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Figure 4-12: TEM cross sectional image of SiCr TFR/TiW junction post trim.

Figure 4-13: The changes in structure of the SiCr film during trim.
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The hypothesis behind the trim process can now be understood as a heating of the film using an electrical pulse. The temperature rise of the film is focused in the centre of the film where the silicon in this area gains enough energy to allow for the electro-migration process. The Silicon atoms will travel towards the anode of the resistor. These Si atoms then come to rest underneath the TiW contact. Similar transport of Si atoms likely occurs in the other direction through thermal-migration caused by the steep thermal gradients induced by the trim. Any Si atoms transported through thermal-migration will be deposited beneath both TiW contacts. The depletion of Silicon atoms in the centre of the resistor results in a larger ratio of Chromium atoms to Silicon atoms. The high temperatures and increased ratio will allow Chromium atoms to diffuse from their original positions to form larger islands which reduce the sheet resistance and increase the TCR. With higher trim pulse amplitudes and/or longer trim pulse times, this process will continue resulting in the Chromium islands growing larger, passing the critical percolation point, and moving closer to becoming a Chromium dominated crystal. Figure 4-13 shows a simplistic planar view of the SiCr film structure during various points of the trim process.

Figure 4-14: TEM planar image of TiW/SiCr junction post trim.
Eventually, as seen in Figure 4-1 and Figure 4-2, the SiCr resistors resistance will start to rapidly increase. Figure 4-14 shows a planar TEM image of the TiW and SiCr film junction after the resistor was stressed to a point where fusing had initiated. In the image, physical tears can be seen in the film which can be attributed to mechanical stress experienced by the film during trim. This mechanical stress is related to the high temperatures and mismatch in thermal coefficients of expansion for the TiW and SiO$_2$ surrounding the SiCr film. As the tears increase, the film will eventually fuse open. The mechanical stress induced during trim needs to be minimised to guarantee the reliability of the resistor during its lifetime of operation.

4.4. SPICE Modelling of SiCr Resistors

At the time of writing, the main model used by ADI for simulation of SiCr resistors is the CMC ET R2 model [2]. This model allows for a non-linear simulation of the resistor. An extra thermal network is available to model non-linearity associated with self-heating. The thermal model can be found below in Figure 4-15.
Prior to the work presented in this thesis, the model used by ADICE contained constants that did not account for systematic errors related to length and did not account for variation in thermal conductivity related to both length and width. Rather constants were used that resulted in inaccuracies for short resistors less than 40 µm in length. The first correction to the model was to account for the systematic errors. A new term $R_{SH_{predicted}}$ was created to account for the systematic error in neighbouring resistors linked to length. The equation defining $R_{SH_{predicted}}$ was based on data from Figure 3-15.

\[
R_{SH_{predicted}} = Rsh \times (1 + (38.4662 \times L^{-1.1693})) \tag{4-3}
\]

Using Equations 3-12 and 3-20 detailed from Chapter 3, the values for $R_{th}$ and $C_{th}$ can be defined as follows in Equation 4-4 and 4-5. This allows for an accurate representation of the thermal dissipation and settling time, which results in improved PCR values generated by the simulator.

\[
R_{th} = \frac{t_{ox}}{G_{tha}. (a. b. \pi) \cdot \frac{1}{t_{res}}} + \frac{(G_{tbp. \text{perimeter}}) + (G_{thc. W. t_{res}})}{} \tag{4-4}
\]

\[
C_{th} = \frac{\rho \cdot c_p \cdot (A_s \cdot t_{ox})}{R_{th}} \tag{4-5}
\]

To allow for trim in the simulator, a $\Delta R_{Trim}$ constant was added to the model. This constant represents the percentage change in resistance after trim. It is defined in the main simulation program before initialising the simulation. If $\Delta R_{Trim}$ is set to zero, this is seen as the initial condition of the SiCr resistor before trim.

\[
R_{SH, post\_trim} = R_{SH_{predicted}} \times \left(1 + \frac{\Delta R_{Trim}}{100}\right) \tag{4-6}
\]

The change in TCR based on $\Delta R_{Trim}$ is calculated from an average fit found in Figure 4-8. This gives an approximate percentage change in TCR for a predetermined, percentage change in resistance.
\[ \Delta TC1_{Trim} = \left( (6.532 \times \Delta R_{Trim}^2) + (8.1988 \times \Delta R_{Trim}) + 5.5921 \right) \% \quad 4-7 \]

The pre-trim value for TC1 is based on the linear relationship found between sheet resistance and TC1 in Figure 3-19 of Chapter 3. This value is then multiplied by the \( \Delta TC1_{Trim} \) percentage change to account for any change in TC1 due to a trim in resistance value. The value for TC2 is based on the highest percentage statistical value for TC2 found in Figure 3-21. The TC2 constant should change with trim, though due to time constraints, limited data were collected to calculate this change. A minor error was expected in simulations associated with this limitation.

\[ TC1 = ((-0.1744 \times R_{sh}) + 162) \times \left( 1 + \frac{\Delta TC1_{Trim}}{100} \right) \quad 4-8 \]

\[ TC2 = 0.025 \ \text{ppm/°C} \quad 4-9 \]

To confirm the accuracy of the model, evaluation data was compared to simulated data of resistors with the same geometry as those resistors from Quad 1, wafer 6 in Table 3-5. The resulting plot of resistance versus dissipated power is found in Figure 4-16. For the ADICE simulation, the Rs term was adjusted to match the measure data from Table 3-5. The corresponding resistance, TCR and PCR values were extrapolated from the simulation and compared to the measured data. For the short 2 \( \mu \text{m} \) and long 80 \( \mu \text{m} \) resistors there were large variations found in the data. But in the mid-range length data there was a good correspondence. The results can be seen in Table 4-1.
Figure 4-16: Simulated results for resistance versus dissipated power for resistors from Quad 1 wafer 6.

Table 4-1: Evaluation data versus simulation data for resistors from Quad 1 wafer 6.
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The variation in PCR between simulation and evaluation data can be accounted as the natural randomness in the TCR versus resistance that is found in Figure 3-19 which shows a sample of resistors sheet resistance versus TCR. The resistor model will be accurate enough to allow for the simulation of a test IC with the accuracy in the trim relying on the characterisation of the final silicon in an evaluation setup.

4.5. X452B: Integrated Trim-able 10kΩ resistor

The X452B test chip was used to test a 16 bit DAC and separately test a cell containing a 10 kΩ resistor that could be trimmed with iTrim. The 10 kΩ cell had a number of requirements. The main requirement was to trim the resistor post assembly to an accuracy of 0.01% and to a TCR of less than 5 ppm/°C. The accuracy requirement of less than 0.01 % was based on the standard capability of LASER trimming as detailed in Table 1-1 in Chapter 2. The TCR value of 5 ppm/°C is a standard value required for precision resistors working with various analogue ICs. This value of TCR would require an external component as no integrated technology exists. The process used for the test chip was a 0.18 µm minimum geometry 5V CMOS process with TFR resistors available between metal 5 and 6. This meant the TFR resistors being approximately 5.5 µm above the silicon substrate. As the test chips main goal was to evaluate the 16 bit DAC, there were also restrictions on voltage supplies, test access and interface control. The supply was a maximum of 5.5 V for final use conditions and 6 V for trim conditions. These were based on the maximum ratings of the 5 V devices used in the IC. There was no availability of a negative supply, only a ground pin which limited the voltage differential to a maximum of 6 V for trim. Test access was available through two general purpose test pins. Multiple signals from the 16 bit DAC and iTrim cell were multiplexed to the test pins. The multiplexing resulted in large parasitic resistances. Therefore, only low current signals could be carried though these pins. The control of access to the test pins and the trim circuitry was through a SPI interface. The final die would be assembled into a 16 lead TSSOP for test. The top level schematic of the test chip can be seen below in Figure 4-17. The 16 bit DAC is in the centre of the schematic and the iTrim cell is to the right of the schematic.
Figure 4-17: Top level Schematic of X452B test chip.
A simple view of the \textit{iTrim} cell can be seen in Figure 4-18. The 10 kΩ resistor consists of two parts. The first is a gross trim cell that contains fuses. The process used for the test chip has a sheet resistance variation of less than +/-6% for the SiCr resistors. This variation was reduced using SiCr fuses as it was too large to trim with the \textit{iTrim} method alone. The fuses reduced the variation in SiCr resistors from +/-6% to +0.6% of a target resistance value. The fine trim cell contains the \textit{iTrim} resistors and is used to trim the absolute value from 0.6% to approximately 0.01% and trim the TCR value from -25 ppm/°C to between +/-5 ppm/°C. Two 4 bit DACs are used to calibrate the 10 kΩ resistor and trim the fuses and \textit{iTrim} resistors. Two test pins are used to sense the voltage across the 10 kΩ resistor. The logic inputs are used to control the 4 bit DACs and various switches.

\begin{center}
\includegraphics[width=\textwidth]{figure4-18.png}
\end{center}

\textbf{Figure 4-18: Simple schematic of a 10 kΩ \textit{iTrim} cell.}
4.5.1. Gross Trim Fuse Cell

As stated previously, the gross trim cell is used to reduce the process variation, related to the sheet resistance, from +/-6% to +0.6% of a target value. The target value for the gross trim cell is approximately 10150 Ω. This is 1.5% above the final target value of 10 kΩ and allows for a window that iTrim can use to reduce the resistance which trims the absolute resistance and TCR values.

In total, there are seven fuse cells. Figure 4-19 shows an individual fuse cell. All resistors and fuses in the cell are SiCr resistors. For each fuse cell the $R_{constant}$ and fuse resistance are kept at the same value and set at 560.1 Ω and 206 Ω respectively. The resistance of $R_{weight}$ is varied for each cell. Under nominal conditions if all fuses are intact the total resistance for the string of fuse cells is 2288.5 Ω. If all the fuses are blown, the resistance of the string increases to 3920.7 Ω (560.1 Ω * 7).

![Figure 4-19: Single fuse cell.](image)
To blow a fuse, the matching switches for the particular fuse are turned on. There is a nominal VDD voltage potential, less parasitic voltage drops, across the fuse. $R_{\text{constant}}$ and $R_{\text{weight}}$ are laid out wide enough to be robust to the high current densities necessary to blow the fuse.

The resistance weight of the $R_{\text{weight}}$ resistor in series with fuse 1 in Figure 4-18, is 4 mΩ or a metal short. If fuse 1 is blown, the resistance of the gross trim string and the 10 kΩ string increases by 58 Ω. The resistance weight of the $R_{\text{weight}}$ resistor in series with fuse 2 in Figure 4-18, is 127.7 Ω. If fuse 2 is blown, the resistance increases by 116 Ω or twice the resistance increase if the first fuse is blown. The increase in weight continues. If fuse 7 is blown, the increase in resistance is seven times 58 Ω or 406 Ω. This guarantees that there is a trim range of (3920.7 Ω -2288.5 Ω ) 1632.2 Ω or 16% of the 10 kΩ resistance. The weighting of resistors gives a total resolution of 58 Ω throughout the range which is 0.58% of the 10 kΩ resistance.

<table>
<thead>
<tr>
<th></th>
<th>nominal +</th>
<th>nominal</th>
<th>nominal -</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i\text{Trim Res}$</td>
<td>1928.3</td>
<td>1753.0</td>
<td>1647.8</td>
</tr>
<tr>
<td>4 x ($i\text{Trim Res}$)</td>
<td>7713.2</td>
<td>7012.0</td>
<td>6591.3</td>
</tr>
<tr>
<td>Shunt res</td>
<td>110.0</td>
<td>100.0</td>
<td>94.0</td>
</tr>
<tr>
<td>Minimum 10 kΩ</td>
<td>10340.5</td>
<td>9400.5</td>
<td>8836.5</td>
</tr>
<tr>
<td>Maximum 10 kΩ</td>
<td>12135.7</td>
<td>11032.49</td>
<td>10370.5</td>
</tr>
<tr>
<td>Trim range</td>
<td>1795.2</td>
<td>1632.0</td>
<td>1534.1</td>
</tr>
<tr>
<td>Trim resolution</td>
<td>64.1</td>
<td>58.28571</td>
<td>54.8</td>
</tr>
</tbody>
</table>

Table 4-2: Resistance of 10 kΩ string under skew conditions.

Table 4-2 shows that, independent of sheet resistance, the $i\text{Trim}$ cell will always have enough range to allow for a fine trim and TCR trim.

4.5.2. Fine Trim $i\text{Trim}$ Cell

As stated in Table 4-2, there are four $i\text{Trim}$ resistors placed in a string configuration with each resistor having a resistance of 1753 Ω. A string of four $i\text{Trim}$ resistors were chosen over a single $i\text{Trim}$ resistor for three reasons. Firstly, the four resistors allow for
greater flexibility in the final resistance value and TCR of the post trim fine trim cell string. Secondly having four matching resistors allows for one resistor to be gross trimmed first and allow the collection of data used to derive the Δ resistance versus Δ TCR graph as shown in Figure 4-9. The final reason is the restriction of voltage potential for the trim. A smaller resistor value requires a lower voltage to deliver the same amount of current as a larger resistor value. A simple diagram of the iTrim fine trim cell is seen below in Figure 4-20. The 4 bit trim DAC allows for the regulation of the VDD voltage potential applied across the iTrim resistors during trim. To trim the resistors the switches associated with a particular iTrim resistor are turned on. For example switch 8a and 8b are turned on if iTrim resistor 1 requires trimming. Likewise switch 9a and 9b are turned on if iTrim resistor 2 requires trim.

![Simple schematic of fine trim cell.](image)

**Figure 4-20: Simple schematic of fine trim cell.**
The concept behind trimming the resistors absolute resistance and TCR is based on the plots in Figure 4-21 and Figure 4-22. Figure 4-21 shows a typical graph for an individual resistor change in TCR versus change in absolute resistance with \(i_{Trim}\). From this plot it can be seen that there is 100% increase in TCR with 5% reduction in resistance value. A 100% change in an individual resistor’s TCR results in a TCR value of 0 ppm/°C. Figure 4-22 shows the same graph but with the x and y axis scaled to the ratio of the 1.75 kΩ \(i_{Trim}\) resistor to the entire 10 kΩ string. To trim the TCR of the entire 10 kΩ string to 0 ppm/°C or 100%, the 10 kΩ resistance needs to be trimmed by approximately 1.75% which is equivalent to 10% of the \(i_{Trim}\) resistor value. If two of the trim resistors in the 10 kΩ string are trimmed individually by 7.5% of their original values, this should result in a 2.6% drop in the 10 kΩ resistance. The third \(i_{Trim}\) resistor can be used to fine trim the resistance value by up to 0.5% of the 10 kΩ resistor. This will not change the TCR by more than 5% of the original 10 kΩ TCR value. If this was originally 25 ppm/°C, then 5% would be 1.25 ppm/°C. To allow for this, the fuses would be used to increase resistance to 10310 Ω prior to trimming the \(i_{Trim}\) resistors. To make sure a precision trim is achieved, the resistor specific plot for Figure 4-22 is generated from the measured data during the trim of the first resistor.

![Figure 4-21: Typical individual resistors Δ resistance versus Δ TCR plot.](image)
Figure 4-22: Trim effect of a 1.75 kΩ resistor on a 10 kΩ resistor string. 

Δ resistance versus Δ TCR plot.

As previously stated, there is a limit of 6 V for the voltage potential available for the trim. Choosing the \( i_{Trim} \) resistor geometry started with the number of \( i_{Trim} \) resistors required. Four resistors were suitable in meeting the requirement of trimming to 0 ppm/°C with a resistance trim window of 0.6%. The value of the resistors is a large enough value to have a significant impact on the overall 10 kΩ string but small enough to be trimmed. A value of 1753 Ω with a width of 2 µm and length of 3 µm was chosen as this value and geometry would allow up to 1.7 mA/µm available for the trim. Typically, for a resistor deposited on 5.5 µm of oxide, a current bias of 1 mA/µm should be sufficient for trim. Figure 4-23 shows the schematic for one of the two 10 kΩ resistors placed in the X452B test chip. The gross trim cell is stacked on top and in series with the fine trim cell. Dummy resistors and fuses have been added to improve electrical and thermal matching.
Figure 4-23: A 10 kΩ Resistor in the X452B test chip.
4.5.3. \textit{iTrim} Test Access and 4 bit DACs

As seen in Figure 4-18, there is a requirement for a number of switches to deliver trim voltages to various points of the 10 k\(\Omega\) resistor string. Due to limited layout time, standardised transmission gates were used for all switches in the \textit{iTrim} 10 k\(\Omega\) cell and for the 4 bit DACs. Performance was not affected but to save silicon area specifically sized individual PMOS or NMOS FETs could be used rather than a full transmission gate. The standardised transmission gate can be seen in Figure 4-24. It consists of an inverter, enable signal and a PMOS and NMOS device placed in parallel to transmit the input signal.

![Figure 4-24: \textit{iTrim} transmission gate.]

The devices mp3 and mn3 were sized to allow for a worse case 350 mV drop across the transmission gate when enabled and sinking or sourcing a load of 4 mA. A simulation of the voltage drop across the transmission gate can be found in Figure 4-25. The variation in voltage drop is related to the variation in resistance as the gate source voltage (\(V_{gs}\)) on the PMOS and NMOS changes. At 0 V the PMOS, whose gate is tied to ground, is off. As the PMOS gate voltage increases to around 0.7 V, or the threshold voltage (\(V_t\)), the PMOS turns on in the high resistance saturation region due to the large drain source voltage (\(V_{ds}\)) across the device. As the \(V_{gs}\) of the PMOS further increases, until its \(V_{ds}\)
voltage is less than $V_{gs}$ minus $V_t$, it moves into the lower resistance linear region and starts to conduct more current than the NMOS until it eventually dominates the resistance of the transmission gate. The reverse happens for the NMOS device in that it starts in the linear region, moves into the saturation region and then turns off. This results in the two hump plot below. The transmission gate will be used to short nodes to ground or close to the VDD voltage therefore typically the transmission gate will be operating in the region from 5 V to 6 V or 0 V to 1 V.

![Plot of voltage drop across transmission gate versus voltage bias on out node for an enabled transmission gate.](image)

In future generations of the transmission gate cell, a better solution would be to use NMOS only devices for the 0 V to 1 V operating region and PMOS only devices for the 5 V to 6 V operating region. Silicon area could be reduced or the area of devices made
larger to reduce voltage drops and therefore require lower VDD voltages to trim the resistors and blow the fuses.

The configuration of the transmission blocks for switching the ground and VDD supplies across the fuses and resistors can be seen in Figure 4-26 and Figure 4-27. As seen in Figure 4-19 and Figure 4-20, there are a pair of switches for each fuse and \(i_{Trim}\) resistors. The bottom transmission gates short nodes of the 10 kΩ string to the ground supply while the top transmission gates short nodes of the string to the VDD supply. If 4 mA was flowing through the fuse or \(i_{Trim}\) resistor, in the trim or fuse blow configuration, these gates would result in a total voltage loss of 0.7 V.

![Figure 4-26: Fuse transmission gates.](image-url)
Figure 4-27: iTrim resistor transmission gates.

Figure 4-28 shows the schematic for the characterisation and trim four bit digital to analogue converters. The DACs in the iTrim cell can be thought of as more load regulators, as the resistance of the DAC is increased to increase the voltage drop across the DAC. Therefore, this reduces the current load or voltage drop across the selected 10 kΩ resistor string.

There are two sets of resistors in the DAC, as shown in Figure 4-28. The first set consists of thin film resistors which are sized to deliver a code dependent current of 167 µA to 440 µA to the 10 kΩ string. The second set consists of poly-silicon resistors which have lower resistance of 1 kΩ per resistor. There will be a lower voltage drop across these resistors. Therefore, a greater current is sunk to the selected individual resistor or fuse. The code dependent current varies between 1.8 mA and 2.7 mA.
Figure 4.28: iTrim integrated characterisation and trim DACs.

For Characterisation:
- Testmode<0> is high
- I range is 18/4A to 440/4A

For iTrim:
- Testmode<1>, Testmode<2>, or Testmode<3> is high depending on which of the 3 resistors is to be trimmed.
- I range is 1.8mA to 2.7mA

Thick metal needs to be 4um wide.
When the thin film resistors are enabled, the low current is used to perform a characterisation sweep across the selected 10 kΩ resistor. To measure the resistance of the 10 kΩ resistor string, a current monitor or shunt would be placed in series with the VDD pin and its voltage supply. This will allow for a current measurement. The voltage drop across the 10 kΩ resistor is measured using a voltmeter across the two sense test points. From the current and voltage measurement, an accurate four wire resistance measurement is made which can be plotted versus the measured characterisation current. Figure 4-29 shows an example resistance versus current plot, where all sixteen codes in the 4 bit DAC are stepped through with a resistance measurement at each code.

![ADICE plot of X452Bs 10kΩ Resistance versus current.](image)

**Figure 4-29: ADICE plot of the X452Bs 10 kΩ Resistance versus current.**

The higher current provided by the poly-silicon resistors allows for a trim current. The polysilicon resistors were used for this portion of the DAC because of their greater current handling capability. An area of future research is the position of the second series transmission gates to connect the poly-silicon resistors in parallel with the TFR resistors. This transmission gate rather could be in series with the TFR resistor as there is lower
current required. Therefore the voltage loss will be minimised. The trim circuit operates by starting the trim pulse with an SPI write and ending with another SPI write. A typical trim pulse of 10 ms is easily achieved.

4.5.4. Digital access to iTrim cell

The SPI interface is a 3-wire data input only configuration. The pins required are data in (DIN), clock (SCLK) and chip select (CSB). The SPI interface accepts a 32 bit input word where data is clocked in on the rising edge of SCLK when CSB is held low. The max clocking frequency is 50 MHz with a logic voltage of 5 V. The format for the SPI register can be seen in Table 4-3.

<table>
<thead>
<tr>
<th>[31]</th>
<th>[30:27]</th>
<th>[26:23]</th>
<th>[22]</th>
<th>[21]</th>
<th>[20]</th>
<th>[19:16]</th>
<th>[15:0]</th>
</tr>
</thead>
</table>

Table 4-3: X452B SPI interface.

This interface is shared with the 16 bit DAC. To make sure that both circuits do not interfere with each other, the MSB is used as the control bit where the MSB needs to be high to access the iTrim functions. The iTrim DAC Code is controlled by bits 27 to 30. This code controls the characterisation DACs main transmission gates. A specific test mode is required to turn on the transmission gates placed in series with the polysilicon resistors to allow for trim or fuse blowing. Codes 26 to 23 control the test mode configuration the iTrim cell is in. Explanations of the various test modes can be seen in Table 4.4. Test modes 1 to 11 are for configuring the various transmission gates to blow fuses or trim iTrim resistors. Test modes 13 to 15 allow for various methods to characterise the 10 kΩ resistor. Test mode 13 is default for characterisation. Bit 22, of the SPI interface, allows for the power down of the 16 bit DAC and the circuitry related to the 16 bit DAC. This results in minimal quiescent current being sourced by the X452B. Bit 21 selects which of the two 10 kΩ resistors are to be trimmed or characterised and
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turns on the transmission gate between the \textit{iTrim} DAC and the selected resistor. The \textit{iTrim} DAC code and \textit{iTrim} test code are common between the two 10 k\(\Omega\) resistors. Bits [19:16] are set to code 15 as a secondary backup to bit 31. Bits 20 and bits 15 to 0 have no effect on the \textit{iTrim} cell.

<table>
<thead>
<tr>
<th>Test mode number</th>
<th>Test Mode Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No effect (default code)</td>
</tr>
<tr>
<td>1</td>
<td>Turn on transmission gates for fuse 1.</td>
</tr>
<tr>
<td>2</td>
<td>Turn on transmission gates for fuse 2.</td>
</tr>
<tr>
<td>3</td>
<td>Turn on transmission gates for fuse 3.</td>
</tr>
<tr>
<td>4</td>
<td>Turn on transmission gates for fuse 4.</td>
</tr>
<tr>
<td>5</td>
<td>Turn on transmission gates for fuse 5.</td>
</tr>
<tr>
<td>6</td>
<td>Turn on transmission gates for fuse 6.</td>
</tr>
<tr>
<td>7</td>
<td>Turn on transmission gates for fuse 7.</td>
</tr>
<tr>
<td>8</td>
<td>Turn on transmission gates for \textit{iTrim} resistor 1.</td>
</tr>
<tr>
<td>9</td>
<td>Turn on transmission gates for \textit{iTrim} resistor 2.</td>
</tr>
<tr>
<td>10</td>
<td>Turn on transmission gates for \textit{iTrim} resistor 3.</td>
</tr>
<tr>
<td>11</td>
<td>Turn on transmission gates for \textit{iTrim} resistor 4.</td>
</tr>
<tr>
<td>12</td>
<td>No effect</td>
</tr>
<tr>
<td>13</td>
<td>Select test mux 1. Test points connected across 10 k(\Omega) Resistor</td>
</tr>
<tr>
<td>14</td>
<td>Select test mux 2. Test points connected across 100 (\Omega) Shunt Resistor</td>
</tr>
<tr>
<td>15</td>
<td>Select test mux 3. Test points connected across fuses and \textit{iTrim} resistors</td>
</tr>
</tbody>
</table>

Table 4-4: X452B test modes explanation.
4.6. Simulated Characterisation of 10 kΩ Resistor

To allow for the accurate trim of both the absolute resistance and TCR of the 10 kΩ resistor string, a simulated characterisation was performed. These calculated coefficients are used in the trim to correct for systematic errors. This characterisation was repeated when X452B devices were available and the resulting coefficients were loaded into the test or probe program.

The first step in meeting the absolute trim was to determine the weight of fuses for a given resistance measurement. This allows for the accurate prediction of the gross trim. Using ADICE, the increase in resistance for a given fuse was simulated for various sheet resistances. Figure 4-30 shows the linear fit for each fuse weight for a given initial resistance measurement. Each linear fit was used to calculate the post trim resistance for a given combination of fuses.

![Figure 4-30: Weight of fuses for a given initial resistance.](image)
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The next step is to establish the relationship between change in resistance and change in PCR for the electrical trim method. Figure 4-31 can be used to calculate the polynomial fit, from which the total change in PCR can be calculated based on the fine resistance trim for the four individual iTrim resistors. The ultimate goal is to have the combination of gross trim and fine resistance trim result in a target absolute resistance value and a target PCR value. The final PCR value should correspond to a 0 ppm/°C TCR.

ADICE was used to calculate an approximate value for the thermal conductivity of the stack which would allow for the computation of the target PCR value for the trim. This was characterised by producing a plot of PCR versus TCR as previously presented in Figure 4-7. Figure 4-32 shows a plot of resistance versus power for the 10 kΩ string. This plot was generated using the same method used for generating the resistance versus current plot in Figure 4-29. From the resistance versus power plot the slope divided by the intercept resistance is taken as the PCR of the resistor at that given temperature.

![Figure 4-31: Change in PCR versus change in resistance.](image.png)
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Figure 4-32: Resistance versus power ADICE plot for the 10 kΩ string resistor.

Figure 4-33: Simulation of PCR versus TCR for a trimmed 10 kΩ string resistor.

The PCR was measured at a number of simulated ambient temperatures to allow for the extraction of the TCR. The resistor model variable deltar was then changed to
simulate the electrical trim of the resistor. After the trim the TCR was again measured. The electrical trim and TCR characterisation was repeated to generate the plot in Figure 4-33. For nominal condition with no blown fuses, the thermal resistivity can be worked out from the slope as 10503 °C/W with an intercept value of 18100 ppm/W. Therefore to achieve a 0 ppm/°C TCR a trim to a PCR value of 241113 ppm/W was needed. Trimming to a PCR value of 0 ppm/W would result in a TCR of around -1 ppm/°C. To assess the effect of blowing fuses on the thermal performance of the 10 kΩ string, the PCR versus TCR plot was produced for individual fuses. It can be seen from Figure 4-33 that the thermal resistivity will change marginally when various fuses are blown resulting in a variation of intercept points which could spread the systematic related trim error by 1 ppm/°C if only a single fit was used in the trim calculations. To further establish the effect of variation in sheet resistance, Figure 4-34 and Figure 4-35 were compiled for two 10 kΩ resistors with a sheet resistance of +3% and -3% of the nominal, shown in Figure 4-33. The thermal resistivity is measured for each resistor and individual fuse combination.

In Figure 4-34: Simulation of PCR versus TCR for 10 kΩ string resistor with sheet resistance of nominal+3%.
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Figure 4-35: ADICE simulation of PCR versus TCR for 10 kΩ string resistor with sheet resistance of nominal-3%.

Figure 4-34 and Figure 4-35 show a variation in required PCR trim for a 0 ppm/°C TCR related to sheet resistance. For a 6% variation in sheet resistance, the target systematic error could be as high as 3 ppm/°C if the variation in sheet resistance and fuse combinations is not accounted for. Figure 4-36 can be used to calculate the true intercept point where the initial 0 ppm/°C equivalent PCR value can be easily calculated based on the initial PCR measurement with no fuses blown. The polynomial fit, from Figure 4-37, is used to calculate the delta PCR value due to specific fuses being blown. The sum of the delta PCR values is added to the initial 0 ppm/°C equivalent PCR value to calculate the true intercept target. This will minimize systematic errors in the trim but not the random errors which will have to be accepted.
Figure 4-36: 0 ppm/°C PCR equivalent versus initial PCR.

Figure 4-37: Change in 0 ppm/°C PCR equivalent value for a given fuse versus initial resistance.
4.7. Simulated Trim of a 10 kΩ Resistor

Using the characterisation data, a program can be written to perform a simulated trim on any variation of the 10 kΩ resistor string within +/-6% of the nominal value. The flow chart in Figure 4-38 is used to perform the trim. To begin, the resistance and PCR is measured. These values get fed into a linear regression program that derives the fuses to be blown and the required trim for each iTrim resistor. The fuses are blown and the first iTrim resistor is trimmed. This initial resistor is used as a control and produces a more accurate fit for PCR versus change in resistance as seen in Figure 4-31. This new plot was used in a second round of linear regression to produce more accurate trim targets for the iTrim resistors. Once the three iTrim resistors are trimmed to the new targets the TCR should be near 0 ppm/°C and the target resistance a few Ohms above 10 kΩ. The final iTrim resistor fine trims the target resistor to 10 kΩ without changing the TCR.

![Flow chart](image)

**Figure 4-38: Precision trim flow.**
Chapter 4: Electrical Trim; Background and Implementation

The linear regression program is a very important part of the trim. It needs to produce an accurate trim target while maintaining an efficient test time. The linear regression flow can be seen in Figure 4-39. The linear regression flow is a brute force method that cycles through the combinations of fuses and \( iTrim \) resistor change that has a post blow resistance above \( 10 \text{k}\Omega \). The time is limited by maximising the step size in the three for loops that calculate the change in resistance for each \( iTrim \) resistor. The method is carried out twice during the trim. A rough fit equation for change in PCR versus change in resistance is used in the first run. The second run occurs when the first \( iTrim \) resistor, being used as a reference, has produced its own fit. Running the linear regression program for the second time minimises random errors and maximises the precision of the trim.

Figure 4-39: Best fuse combination and \( iTrim \) trim calculation using linear regression.

The precision trim flow and regression method were implemented in ADICE to approximate the lowest TCR achievable. Figure 4-40 shows the resulting TCR for a \( 10 \text{k}\Omega \) resistor with an original resistance of \( 9789.3 \text{\Omega} \). The standard TCR measurement
results in a TCR of 3.5 ppm/°C. If the temperature range is reduced to between -40 °C and 125 °C, the TCR specification is reduced to 2.2 ppm/°C. The TCR is limited by the bow in the plot. To minimize the bow, the original TCR will need to be lower. For this test chip and for the SiCr technology used (TCR typically equals -25 ppm/°C) \( i_{\text{Trim}} \) would be limited to approximately 3 ppm/°C over the typical industrial temperature range of -40 °C and 125 °C.

**Figure 4-40: Post trim resistance versus temperature plot.**
4.8. X452B Pin-out and Layout

The pin-out of the 16 pin TSSOP can be seen below in Figure 4-41.

![Figure 4-41: X452B 16 lead TSSOP pin out.](image)

The \textit{iTrim} resistor is connected between \textit{vdd} and \textit{agndf}. TP1 and TP14 indicate the test-pins used to sense the voltage across the resistor. The top level schematic and layouts can be seen in Figure 4-42 and Figure 4-43.

In Figure 4-43 the poly-silicon and TFR 4 bit DACs circuitry can be seen on the far left. The fuses and weighted resistors form the centre left. The 560 $\Omega$ constant resistors used in the gross trim cell are on the centre right. To the right of the large matrix of 560 $\Omega$ resistors are an array of small \textit{iTrim} resistors. Surrounding the gross trim and fine trim resistors and fuses are the various transmission gates used to trim the 10 k$\Omega$ resistors. The fuses and resistors that form the two 10 k$\Omega$ resistors are placed in the centre of the various resistor arrays. At each side is a dummy to improve matching between the two resistor strings.
Figure 4-42: Top level schematic of X452B iTrim cell.
Figure 4-43: *iTrim* top cell Layout.
4.9. Discussion

In this Chapter, a detailed review of the electrical trim method was presented. Experimental data from simple single resistors of various widths and lengths resulted in a detailed understanding of the effects of SiO$_2$ thickness and resistor geometry on the trimming process. It was found that a thinner oxide resulted in a higher current density to trim the resistor. This higher current density resulted in a greater rate in decrease of resistance with trim. These data, along with TEM images, supported the migration of Si atoms from the centre of the resistor through electro-migration.

Based on the simple equations for the change in resistance versus change in PCR an ADICE model was developed to simulate the trimming process. This model was used to design a test chip containing a 10 kΩ resistor string. To allow for the post assembly trim of a 10 kΩ resistor's absolute resistance and TCR, transmission gates and control logic were added to the test chip. A test methodology was then developed to minimise systematic errors. This resulted in a 10 kΩ trimmed in simulation to 3 ppm/°C and to an absolute resistance tolerance of 0.01%.
4.10. Bibliography


5. X452B 10 kΩ Resistor Characterisation and Trim.

In this Chapter the 10 kΩ resistors of the X452B test chip are used to demonstrate the successful trim of both TCR and absolute resistance. To start an overview of the test system is given. The test system uses a number of resources from the simple resistor test system reviewed in Chapter 3. Using the test setup the X452B will be evaluated to allow for the development of the trim program. This trim program will be based on the test flow demonstrated using ADICE in Chapter 4 and will prove the methodology of the trim. Once the successful trim is demonstrated a review of data from reliability tests of trimmed units will be presented to understand how to minimise the drift of absolute resistance over the resistors operational lifetime. Results from humidity and mechanical reliability tests will also be presented to prove the robustness of the trim technology. Optical images of the X452B die and iTrim cell can be seen in Figure 5-1 and Figure 5-2.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

Figure 5-1: Optical image of X452B die.

Figure 5-2: Optical image of iTrim Cell.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

5.1. X452B Characterisation Setup

The test setup comprises of an accurate DC supply to support power for the X452B, a 3458A meter for voltage measurements, an Aardvark SPI host for communications and a number of relays to switch between signals. The test setup supported the characterisation, trim and test of the X452B devices. A simple schematic of the test setup can be found in Figure 5-3. The VOUT supply is the same AD5791 DAC based supply found in Figure 3-7 in Chapter 3. This supply was used due to its low noise, stability and convenience. The Vout supply is buffered, using an AD8676 Op-Amp, to the VDD pin of the TSSOP socket. A Vishay Z-foil 1 kΩ [1] shunt resistor is placed in series between the output of the buffer and the VDD pin. This is to allow for a current measurement. A shunt resistor of resistance 1 kΩ is used as it improves the accuracy of low current measurements. The ground supply is buffered through the AGNDF and AGNDS pins to allow for a more stable and consistent ground supply voltage with variable current loads.

Communication between control PC and X452B is provided through an Aardvark SPI Host Adapter [2]. The PC is connected to the Aardvark with a USB cable and the Aardvark communicates to the X452B through the SPI protocol. The three pins on the X452B that are used in communicating are individually connected to relays. These relays connect the SPI pins to the Aardvark when communicating but when the 3458A is measuring voltage the SPI pins are tied to ground through the relays. This is done to minimise noise and current loss through the communication pins during measurement. All relays within the schematic are controlled using an Arduino UNO microcontroller board [3]. The AD5791A power supply, 3458A meter, Aardvark and Arduino are controlled through the use of a Labview program for all tests.
Figure 5-3: Simple schematic of X452B test setup.

Figure 5-4 shows the X452B evaluation board. To carry out temperature testing, a nylon board with a square piece in the centre cut out for the socket, is placed on top of the evaluation board. This allows the Thermostream to make good contact and regulate the temperature of the part in the socket. To measure temperature a PT100 temperature sensor [4] is taped to the top of the X452B package. The temperature sensitive resistance is then measured using an Agilent 34401A multi-meter.
5.2. Resistance Measurement

To perform an accurate resistance measurement, the flow chart in Figure 5-5 is followed. The X452B is placed in a low power mode using the power down feature. This results in the 16 bit DAC and related circuitry being disabled and pulling minimal current. Code 0 is written to the iTrim 4 bit DAC to make sure no current is flowing through it. Test mode 13 connects the test points to the top and bottom of the 10 kΩ string. A voltage measurement is first performed across the shunt resistor. With the shunt resistance previously characterised to ideally 1 kΩ, the quiescent current can be calculated. This is the minimum current pulled by the part due to leakage and other devices that may by default be pulling some current. The quiescent current also included any errors due to
thermal EMF voltages generated in any thermally mismatching metal junctions between the 3458A meter and the ends of the shunt resistor. Nominally, this current is measured to be 36 µA. The next step measures the voltage across the test points of the X452B. The voltage measured in this configuration is the result of thermal EMF voltage, as no current is flowing through the resistor string. This voltage is recorded as $V_{emf}$ and has a nominal value of 1 µV. Once $i_q$ and $V_{emf}$ are calculated, the X452B can be configured with the desired bias current for the resistance measurement using a specified DAC code. The resulting bias current, $i_b$, is calculated from a voltage measurement across the shunt resistor. The true bias current flowing through the 10 kΩ resistor string is calculated as $i_b - i_q$. The voltage $V_r$, is measured across the test points and from this the $V_{emf}$ voltage is subtracted. The accurate resistance can then be derived from equation 5-1.

\[
R_x = \frac{ib - iq}{V_r - V_{emf}}
\]  

5-1

This method for resistance calculation results in minimal error but it is time consuming. To minimise the extra time required the $i_q$ and $V_{emf}$ measurement can be carried out once before a sequence of measurements. Assuming the ambient temperature stays reasonably steady over the measurement time there will be a limit to any additional measurement errors related to variation in thermal EMF voltages and quiescent current.
5.3. Trim method

The control of the electrical trim is dependent on the amplitude and the width of the voltage pulse used. To minimise trim test time, the pulse width is kept to a nominal time of 10 ms. The width of the pulse is fixed while the amplitude is gradually increased during the trim process. Invariably it may be possible to maintain a high pulse amplitude and gradually increase the width of the pulse. The disadvantage of this method is that the trim junction temperature is always extremely high. This high temperature will induce the Si migration necessary for the trim but it may also activate other changes to the SiO₂ or metal interconnect in the stack. If the pulse width is maintained while the amplitude is
varied, the junction temperature will be maintained to lower levels. Therefore, it should increase the reliability of the post electrically trimmed resistor.

To improve the accuracy of the trim, it is necessary to increase the resolution of the trim DAC. If VDD is kept constant the trim resolution is 1/16th of the VDD voltage. To improve the resolution, the AD5791 DAC used in the power supply is adjusted between the codes of the 4 bit DAC. The adjustment is made in steps of 0.001 V. If the supply is 6 V, this means a 14 bit DAC would be suitable in a production environment rather than the AD5791. To maintain the linearity of the increasing voltage drop across the 10 kΩ resistor, a calibration was carried out, as shown in Figure 5-6.

![Figure 5-6: High resolution trim DAC calibration.](image-url)

Figure 5-6 assumes a base VDD value of 4.5 V from which the AD5791 increases from. This increase is termed as ΔVDD and steps from 0 V to 0.8 V as the 4 bit DAC code changes. By working out a linear sequence between the increase in VDD voltage and the change in 4 bit DAC code, a linear increase in voltage drop across the 10 kΩ resistor can be achieved. Figure 5-7 shows the approximate trim current based on a high resolution trim DAC code and a base voltage of 4.5 V. Figure 5-8 shows the gradual change in resistance and PCR as the trim DAC code is increased from code 1500 to code...
2531 which is the full scale code. The linearity of the high resolution trim code will vary between parts due to the mismatch in the 4 bit DAC but this is irrelevant as the change in resistance and PCR with trim, is always in a single direction.

**Figure 5-7**: Approximate trim current versus high resolution trim DAC code.

**Figure 5-8**: Change in resistance and PCR versus high resolution trim DAC code.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

5.4. X452B Characterisation and Trim

As described in the simulated characterisation section of chapter 4, there are a number of characterisation data points needed for the trim test program to allow for an accurate trim. This characterisation data is generated using the X452B characterisation setup. The data is programmed into Labview which is then capable of calculating fuse codes and trim values that achieve the target absolute resistance and TCR values. This section will present the process of characterising the X452B, followed by successful trim of the 10 kΩ resistor.

5.4.1. X452B Characterisation

The first task in the characterisation is to generate an accurate PCR measurement. Using the flow chart of Figure 5-5, all fifteen codes from the internal characterisation DAC were used to produce the resistance versus power plot of Figure 5-9. To minimise test time, only codes 1 and 15 were used to calculate the PCR value in the final trim program.

![Example resistance versus power plot using X452B evaluation setup.](image)

Figure 5-9: Example resistance versus power plot using X452B evaluation setup.
The initial piece of data required for the trim program is the approximate weight of fuses for a given initial resistance. Figure 5-10 presents the fuse weight based on data collected from a number of X452B devices. The results show around 14% increase over the simulation results in Figure 4-30. This indicates that the fuses have a lower resistance or that the constant value resistors have a higher resistance than expected. Due to the large size of the constant resistors, it can be assumed that the short fuses are resulting in a lower than expected resistance.

![Graph of fuse weight versus initial resistance.](image)

**Figure 5-10: Fuse weight versus initial resistance.**

The accuracies of the fuse codes are important as they limit the resistance error between the predicted values in the linear regression program and the actual values. The resistance error can be corrected for, but the prediction error can result in an error in the final TCR value.
The initial linear regression program bases the target change in PCR to achieve a 0 ppm/°C TCR value on Figure 5-11 and Figure 5-12. Figure 5-11 plots the measurement results of PCR versus TCR for five X452B units. Each unit measurement is comprised of sixteen to nineteen individual TCR measurements. With each TCR measurement taking approximately thirty minutes, the overall measurement took approximately twelve to thirteen hours. Due to the long duration of the measurement and the variability of the ambient temperature in the lab there was a reduction in measurement accuracy. Therefore the resulting tolerance was +/- 2 ppm/°C. The large error tolerance resulted in a minimal fit for the measured data in Figure 5-12. If the measured data is compared to the simulated data of Figure 4-33 a good correlation in terms of the initial PCR and the slope is obvious. If the slope from the simulated data is used in the characterisation data, a better approximation of the required intercept PCR value is achieved.

Figure 5-11: TCR value for a given PCR/R value during the trimming process.
Figure 5-12: Target intercept PCR value that is equivalent to a TCR of 0 ppm/°C versus initial PCR.

By calculating the difference between the initial PCR value and the intercept PCR value, the total required change in PCR is found. The impact on PCR related to fuses blown was not characterised due to the complexity of evaluating this, so the fits from simulation were used as presented in Figure 4-37. Using the polynomial fit in Figure 5-13 the required change in resistance can be calculated for each \textit{iTrim} resistor. This in turn results in the desired change in PCR. This polynomial fit can be calculated using the first \textit{iTrim} resistor to achieve more accurate trim values and TCR closer to 0 ppm/°C.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

Figure 5-13: X452B Characterisation data of Δ PCR versus Δ Resistance.

The final test program combined the following data points to allow for a fast, reliable and repeatable trim.

- The increase in resistance related to blowing a fuse in Figure 5-10
- The linear fit of Figure 5-12 related to calculating the required change in PCR to achieve 0 ppm/°C
- The polynomial fit of Figure 5-13 used to calculate the change in resistance for each iTrim resistor.

5.4.2. X452B Trim

To trim the 10 kΩ string resistors the test program followed the flows presented earlier in Chapter 4 and shown in Figures 4-38 and 4-39. The characterisation data acted as the base for the linear regression method. A simple example of the trim can be seen below. Beginning with an untrimmed resistance and PCR values of 9500 Ω and -
250,000 ppm/W respectively, the regression program will be run to determine what fuses to blow to increase in resistance to allow for the required drop in resistance that trims the TCR to 0 ppm/°C. If it is assume that post fuse blow, the resistance has increased to 10300 Ω and the PCR is now -230,000 ppm/W, the polynomial fit from Figure 5-13 is used to find the required trim values for each of the \( i_{Trim} \) resistors. The chart in Figure 5-14 uses this polynomial fit to select four resistance trim values that decrease the resistance by 300 Ω and increase the PCR by 230,000 ppm/W plus 40,500 ppm/W. The value of 40,500 ppm/W is the intercept PCR derived using Figure 5-12. The initial three resistance values are selected as -140 Ω, -110 Ω and -40 Ω which have equivalent PCR values of 155000 ppm/W, 95000 ppm/W and 17500 ppm/W. This results in a resistance change of 290 Ω and a PCR change of 267,500 ppm/W which ideally would result in a resistance of 10 Ω above the resistance target and the PCR under trimmed by 230,000 + 40,500 = 3000 ppm/W. The fourth and final \( i_{Trim} \) resistor can then trim the resistance by 10 Ω and arrive at the desired 10 kΩ value while also doing a slight trim of the PCR to bring it to the desired intercept value equating to 0 ppm/°C.

![Figure 5-14: Selecting resistance values to achieve a required PCR value.](image)
If the TCR was measured during the trim process the measurements could be combined to produce Figure 5-15.

![Figure 5-15: Resistance versus temperature measurements during trim process.](image)

The final TCR should result in a near TCR value centred at the trim ambient temperature which is nominally 25 °C as seen in Figure 5-16.

![Figure 5-16: Final Resistance versus TCR plot.](image)

The main focus of the trim implementation was centred on making the trim not only accurate but as fast as possible. If iTrim was to be released as a commercial method, then
any reduction in trim time would result in higher profit margins for the post trim resistor, which would in turn increase the use of the technique in various ICs.

Figure 5-17 shows two simple plots of the voltage amplitude used for blowing a fuse and trimming an $i_{Trim}$ resistor plus the effect on the resistance of the 10 kΩ string. For the X452B, the time required to blow each fuse using the maximum current available from the buffer amp in the characterisation setup, was 6 seconds. This was due to the current limits of the buffer. When the X452B was placed on an industrial standard probe station, the fuse was blown in approximately 50 ms as the supply had a much greater current range. The $i_{Trim}$ pulse duration, as previously mentioned, was 10 ms while the measurement time was approximately 0.5 seconds per resistance measurement. The measurement time was restricted by the setup times and read times of the 3458A.

![Figure 5-17: Simple signals plot of trim method.](image-url)
The accuracy of the measurement required is 16 bits which equates to a resolution of 0.15 $\Omega$ for a 10 k$\Omega$ resistor. The measurement time for 16 bits is significant using the 3458A and would not be commercially viable. To reduce measurement time, the voltage across the shunt resistor and the test points could be amplified and subtracted from each other as found in Figure 5-18.

Figure 5-18: Fast measurement schematic.
In Figure 5-18, approximately the same current is flowing through the 10 kΩ shunt resistor as the internal 10 kΩ array. Using the AD5541 DAC, an offset can be added or subtracted to the inverted and 2x gained shunt voltage to account for any quiescent current in the X452B. The positive shunt voltage is then subtracted from the 2x gained voltage drop across the test points to produce a single V_res voltage, which represents the resistance ratio between the internal 10 kΩ and the shunt 10 kΩ. This test configuration halves the voltage measurements required to produce a single resistance measurement while also reducing the measurement resolution to 14 bits which would result in a measurement resolution of 0.3 Ω. The reduced requirements would reduce a resistance measurement from 0.5 s to around 10 ms.

The final system related addition to the test time is the time required to communicate between the X452B and the PC. The current X452B test setup restricts the SPI clock to 20 kHz. But the main delay is the switching time required for the relays which is typically 10 ms. The sum of the various communication component results in a communication time of 32 ms. To reduce this time on the test system the relays would be removed as the industrial system would be capable of putting the communication signals to ground. Then if the same 32 bit word was used with a max frequency of 50 MHz the trim and measurement communication durations would be reduced to a single micro second each and therefore make the write time irrelevant to the total trim time. But for a conservative estimate the communication time will be stated as 1 ms.

To further minimise the trim time an efficient algorithm, needed to increase the voltage amplitude while trimming, is required. As seen in Figure 5-8 there would be typically 750 codes to sweep through to \( i_{Trim} \) the resistance by 150 Ω. With a trim pulse of 10 ms plus 1 ms for communication and 10 ms for measurement the 750 codes would result in a trim time of 15.75 seconds per \( i_{Trim} \) resistor. Figure 5-19 shows the change in resistance for a given trim code when the trim code is stepped up one code at a time or at a rate of 10 codes at a time. It can be seen from the plot that stepping at a higher rate
results in a lower change in resistance. This is due to the max change in resistance for a given code is not reached in the 10 ms trim pulse time so if a larger number of pulses are applied between two trim codes a bigger change in resistance will result. Figure 5-20 applies two linear fits to each trim code step range plot. For the 1x step range initially, 8.6 trim codes are required to achieve a single Ω change. This reduces to 2 trim codes when the point of critical percolation has been reached. For the 10x step range the initial requirement for a single Ω change in resistance, is 10.6 codes which reduces to 2.5 codes again once the point of critical percolation has been reached. It can be assumed that the 1x step range has the lowest number of codes required for a given resistance change and that if a lower number of pulses is stepped between codes then the rate of change from the 1x step will not be exceeded.

Figure 5-19: Trim code versus resistance change with trim code increase in steps of 1 or steps of 10.
Figure 5-20: Linear fits of trim code versus resistance change with trim code increase in steps of 1 or steps of 10.

$$y = -2.465x + 1442.7$$
$$y = -2.0028x + 1384.9$$
$$y = -8.5996x + 835.71$$
$$y = -10.579x + 935.55$$

Figure 5-21: Flow chart of trim code increase with change in resistance.
From the data in Figure 5-19 and Figure 5-20 a trim pulse algorithm can be produced that follows the flow chart depicted in Figure 5-21. Using the algorithm an average of 25 pulses are required per resistor to arrive within 1 Ω of the target resistance. This results in a maximum trim time of 2.1 s for the four iTrim resistors. To calculate the entire time required to trim the 10 kΩ resistor, the 2.1 s for trimming the iTrim resistor is added to the time required to blow the fuses. It is believed that using a production test system the full process will be complete in a worst case time of 2.5 seconds.

Figure 5-22 shows some examples of post trim resistors. The resistance tolerance is found to be +/- 0.02% of 10 kΩ at 20 °C. The tolerance would be tighter only for a slight change in resistance once the trimming process is complete. The drift is likely related to the relaxation of the thermally heated resistors during trim. This usually results in a negative shift though there are some units which shift in the positive direction. Therefore, the drift cannot be accounted for in the trim process. Despite this drift the tolerance of the resistor makes it competitive with LASER trim. Figure 5-23 depicts the percentage change in resistance versus temperature. From this plot, it can be seen that the variation for a particular resistor is never more than 3 ppm/°C. The TCR could be reduced if centred correctly, but the inaccuracies in the trim results in a variation related to over trim and under trim between various units. Even with the variation the results demonstrate a successful method in a high accuracy trim of both absolute resistance and TCR post assembly.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

Figure 5-22: Resistance versus temperature plots for post trim resistors.

Figure 5-23: Resistance change, with respect to resistance at 20 °C, versus temperature.
5.5. X452B Reliability Testing

The target market for *iTrim* technology is industrial, automotive and medical. All applications in these markets require high reliability over lifetimes of up to 10 years. To assess the durability of the post trimmed resistor, a number of reliability tests were carried out. These tests stressed the resistor electrically and mechanically with the drift in absolute resistance set as the indicator for failure. Each test contained untrimmed resistors acting as controls. Controls were kept at the electrical test site to confirm that the measurement equipment had not changed between tests. The measurement equipment used was the X452B characterisation setup reviewed earlier in this chapter. The drift measured in the various experiments were combined together to allow for prediction of total drift over the lifetime of the part [5]. The tolerance change over lifetime can affect precision of the resistor as seen in Figure 5-24. System designers need to account for the end of life tolerance, as this is level of performance variation that the system will experience.

![Figure 5-24: Drift in precision tolerance over lifetime.](image-url)
5.5.1. Lifetime Drift Testing

Lifetime testing or high temperature operating life testing (HTOL) is a standard test used in Analog Devices and the wider semiconductor industry [6]. HTOL consists of biasing the device for test, in this case the 10 kΩ resistor in the X452B, and placing the device into a high temperature oven. The bias applied to the resistors needs to be at least 10% above the expected bias in the final application. The combination of high temperature and high current density results in an acceleration of failure modes such as thermal-migration and electro-migration for a resistor under test.

HTOL of X452B units was performed on a high temperature rated HTOL board. The HTOL board was specific for the X452B and allowed for five individually configured groups. Devices in each group were connected in parallel, using the SPI protocol, to the control PC. The HTOL board can be seen in Figure 5-25.

![Figure 5-25: X452B HTOL board.](image)

The HTOL board was loaded into a HTOL oven which contained a backplane containing power supplies and digital inputs. An X452B specific program was set to
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

supply a VDD bias of 5.5 V. The SPI interface would be used to configure the internal four bit characterisation DAC in the iTrim cell, to allow for a specific current density. The parts would be pulled at fixed intervals and tested using the X452B characterisation setup. Typically, testing consists of 1000 hours in the oven at 125 °C. Using the Arrhenius equation and a general activation energy of 0.7 eV, the accelerated test period of 1000 hours is found equivalent to 10 years operation at a maximum temperature of 53 °C [7]. This can be seen below in Equation 5-2.

\[
A_T = \exp\left( \frac{-E_a}{k} \left( \frac{1}{T_{test}} - \frac{1}{T_{use}} \right) \right) = \exp\left( \frac{-0.7}{0.000086} \cdot \left( \frac{1}{273 + 125} - \frac{1}{273 + 55} \right) \right) = 77.6
\]

Where:

- \(A_T\) = Acceleration factor.
- \(k\) = Boltzmann’s constant (8.6173324 x 10^{-5}.eV.K^{-1}).
- \(T_{test}\) = Test temperature in Kelvin.
- \(T_{use}\) = Use temperature in Kelvin.
- \(E_a\) = Activation Energy in eV.

All testing carried out in the HTOL oven was performed at 125 °C unless otherwise stated. A picture of a HTOL oven can be seen in Figure 5-26.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

The first evaluation was designated X452B1 and aimed to investigate the drift of resistors trimmed by different resistance amounts. Figure 5-27 shows results for group 1 of reliability evaluation test X452B1. All four \textit{iTrim} resistors in unit 4 of group 1 were trimmed by 5 Ω. The remaining 10 kΩ resistors had each of their \textit{iTrim} resistors trimmed by different amounts as indicated in Table 5-1. All units are listed in detail in Appendix 2.

<table>
<thead>
<tr>
<th>Unit Number</th>
<th>Resistance Trim</th>
<th>Number of \textit{iTrim} resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>5 Ω</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>30 Ω</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>50 Ω</td>
<td>4</td>
</tr>
<tr>
<td>7</td>
<td>60 Ω</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>80 Ω</td>
<td>4</td>
</tr>
<tr>
<td>9</td>
<td>150 Ω</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>200 Ω</td>
<td>4</td>
</tr>
</tbody>
</table>

\textbf{Table 5-1: Resistance trim for a given unit.}
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

All resistors were biased with a load of 550 µA in the HTOL oven for a duration of 500 hours. The results from group 1 show a larger drift for a larger resistance trim. The majority of drift occurred in the initial 168 hours followed by a minimal drift between 168 hours and 500 hours. This indicates that the drift mechanism saturates post 168 hours and is heavily dependent on the electrical trim. As the drift looked to be at 0.1% after 1000 hours, it was decided to analyse if some of the drift count be neutralised during the trim process. To do this, a high amplitude current pulse was applied to each iTrim resistor post electrical trim. The drift correction pulse was not as high of a voltage amplitude as the final trim pulse applied to the iTrim resistor. Despite this, it was significant enough to heat and anneal the post trim resistor. The 10 kΩ string resistor's resistance was found to increase by a few Ohms post anneal. In Figure 5-28, the drift results from five separate groups are presented. The second group, units 11 to 17, have been trimmed in the same order as group 1 and are shown in Table 5-1. A post trim anneal pulse of approximately 2 mA has been applied for two seconds to each iTrim resistor in the group. Group three, units 18 to 24, have had the same trim as group 1 followed by an electrical anneal pulse of approximately 2 mA for a duration of 5 seconds to each iTrim resistor. Groups four,
units 25 to 31, and five, units 32 to 38, are replicas of groups two and three in terms of trim to \( i_{\text{Trim}} \) resistors but have all their fuses blown.

![Graph](image)

**Figure 5-28**: X452B1 results, groups 1 to 5. Test conditions per Appendix 2.

The effect of the post trim anneal pulse clearly shows a halving of drift over the 500 hours test period. Some of the initial drift found in group one parts has been induced during the trim process, creating a more stable resistor in the final application. To allow for a precision trim, including an anneal pulse, the trim process is modified to apply the trim pulse after the initial three \( i_{\text{Trim}} \) resistors are trimmed. The increase in resistance resulting from the anneal pulse is then corrected for using the fourth and final \( i_{\text{Trim}} \) resistor which should only have to decrease resistance by a few Ohms. The anneal of the fourth \( i_{\text{Trim}} \) resistor does not increase the resistance significantly and therefore does not affect the accuracy of the trim.
Figure 5-29: HTOL testing of trimmed 10 kΩ resistors. Test conditions per Appendix 2.

Figure 5-29 shows the final data points from the X452B1 lifetime evaluation. These nine parts were trimmed to 10 kΩ and to a low TCR nearing 0 ppm/°C. The units were then stressed to 1000 hours with a current load of 500 µA. Data clearly shows that the drift over the resistors application lifetime, due to a worst case load, will typically be 0.03% of the absolute resistance.

5.5.2. Humidity and Mechanical Testing

To evaluate the effect of the system manufacturers PCB assembly process on the specifications of the 10 kΩ resistor, a preconditioning test was performed. This test consists of baking the devices for 24 hours to drive out any moisture within the TSSOP moulding compound. The devices are placed into a humidity chamber unbiased and sitting on a metal tray. The level of humidity and duration in the chamber is specified by the moisture sensitivity level (MSL) of the part is to be qualified to [8]. Once the devices have reached the specified time in the humidity chamber, they are placed on a PCB
without solder and put through a reflow oven which can reach temperatures of up to 260 °C. The plastic package would have absorbed a lot of moisture prior to reflow, resulting in a large instantaneous mechanical stress on the die as the moisture is evaporated when the device travels through the reflow chamber. This test replicates the assembly process for the part, in that when the parts are sold they will be sitting in storage waiting for assembly. During this wait, the devices will soak up moisture from the natural environment. Once the parts are ready to be put through a reflow oven for assembly on to the PCB, the manufacturer needs to know if they need to bake the parts prior to the reflow process. This bake step is used to drive out moisture. This is an added cost for manufacturers so it is preferred if the device has an MSL rating of 1. This is the highest rating and allows for the part to be stored for an unlimited duration prior to reflow. The MSL rating is determined by the drift experienced by the resistor during the MSL 1 or the lower rated MSL 3 reliability test. If the drift is satisfactory in the MSL 1 reliability test, the part can be rated MSL 1. The MSL 1 reliability test requires 168 hours in the humidity oven with 85 % relative humidity and an ambient temperature of 85 °C. The MSL 3 testing requires 192 hours in a humidity oven at 60 % relative humidity and 30 °C.

![Graph](image)

**Figure 5-30: X452B5 precondition evaluation data. Test conditions per Appendix 2.**
Figure 5-30 shows the results for evaluation X452B5. X452B5 consists of three groups with each group having the same trim as detailed in Table 5-1. Group 1 comprised of units 4 to 10, group 2 comprised of units 11 to 17 and group 3 comprised of units 18 to 24. Units 1 to 3 were untrimmed controls placed into the humidity chamber with the test units while units 31 to 33 were controls kept beside the characterisation test system. All units had a post trim anneal pulse applied. Both groups 1 and 2 were tested using the MSL 1 conditions while group 3 units were tested with MSL 3 conditions. The data shows that post preconditioning all units experienced a similar amount of drift relative to the resistance trim applied. This drift was significant at a maximum of 0.035% of the absolute value. All units were then placed into a HTOL oven to analyse if the drift experienced in the initial 168 hours for the X452B1 units was added to the drift from preconditioning. What data show is a small additional drift after 168 hours. This points to the thermal conditions experienced in the initial 24 hours bake. The humidity chambers induce the same drift as the conditions in the initial 168 hours drift of the X452B1 units which had not experienced preconditioning. If data are combined from the precondition and lifetime load conditions, a maximum of 0.035% drift from the assembly process can be expected. If it is assumed that the assembly process has eliminated the initial drift then the load conditions will only result in 0.015% drift. Total drift can then be taken as a maximum of 0.05% of the initial absolute resistance, over the lifetime of the resistor.

Other than the load conditions and assembly related drift, causes of drift can be related to mechanical stress from ambient temperature change and prolonged humidity exposure. Typically, industrial and automotive parts can have a temperature operating range of -40 °C to 85 °C. In applications such as automotive, it is very plausible that the part will need to function across this temperature range over the device lifetime, if for example, the device is installed in the engine bay. To test for these conditions a temperature cycle test is carried out. The most extreme test conditions available are 500 cycles of ambient change from -65 °C to 150 °C [9]. The duration of the cycle is
30 minutes with the unbiased part experiencing -65 °C for approximately 5 minutes and 150 °C for 5 minutes. The remaining time is used to ramp the ambient temperature. Additional to the causes of drift is a prolonged exposure to humidity. As detailed in the precondition test of the TSSOP’s non hermetic plastic, humidity can be soaked up into and held by the molding compound. This results in moisture slowly reaching the top of the die and corroding the metal interconnect and the SiCr resistor which is placed high up in the stack. The appropriate test used to evaluate drift due to humidity is a highly accelerated stress test or HAST. This test exposes a biased part to a temperature of 130 °C with a humidity of 85% [10]. The high temperature and humidity produces a build-up of pressure, which is regulated to 2 atmospheres.

![Figure 5-31: X452B7 TCT and HAST evaluation results. Test conditions per Appendix 2.](image)

Figure 5-31 shows results from evaluation X452B7. In this evaluation, four groups, where the resistance was trimmed per Table 5-1 were first put through the precondition
flow which resulted in drifts of up to 0.03%. Two groups were then placed through HAST and temperature cycling. From Figure 5-31, it can be seen that both HAST and TC resulted in a maximum of 0.01% additional drift. When this drift is added to the 0.05% drift related to load conditions and the assembly process, a total lifetime drift specification of 0.07% is derived. This lifetime specification is very competitive with current technology which can be greater than 0.1% [5].

5.6. X452B TEM Analysis

To examine the SiCr resistors to assess if there was any damaged experienced during the trimming process a TEM analysis was used to carry out a visual inspection. Two lamellae were prepared from the same die. Each lamella contained a post trim resistor from the X452B. The first resistor was trimmed by 10 Ω and the second by 120 Ω. The positions of the lamellae can be seen below in Figure 5-32 with the first lamella already removed using a FIB and the second highlighted with the green box.

Figure 5-32: SEM images of lamella positions.

Figure 5-33 shows the TEM images for the resistor trimmed by 10 Ω. The top image shows one of the TiW contacts and a portion of the SiCr film. Two boxes highlight the
position of the lower higher resolution images. From the figures no obvious thermal changes have occurred with a 10 Ω trim. The SiCr film looks to be of consistent thickness and there is no appearance of a Silicon deposit.

The second lamella contains the resistor trimmed by 120 Ω. The TEM images for the second lamella can be found in Figure 5-34. The top image shows the sites for the high resolution images placed below. The SiCr film again looks to be consistent but the TiW contact does show evidence of a Silicon deposit under the TiW contact. This correlates with the earlier TEM images of Figure 4-12. The lack of any thermal damage further supports the robustness of the resistor confirmed in the reliability tests.

![Image](image.jpg)

**Figure 5-33:** TEM of X452B iTrim resistor with a trim of 10Ω.
5.7. Discussion

In this Chapter a test setup was described that allowed for evaluation of the X452B test chip. The bench setup allowed for the characterisation of the PCR versus TCR relationship together with the PCR versus Δ resistance correlation. This data was used to finish the trim test program. Using this bench setup together with the test program, the 10 kΩ resistor’s absolute resistance and TCR were successfully trimmed using a combination of SiCr fuses and resistors arranged for iTtrim. Below, in Table 5-2, a list of the important specifications for the 10 kΩ resistor is presented. The post trim tolerance of
the TCR trim is found to be 3 ppm/°C with an absolute trim tolerance of 0.02%. Because the width of the resistor needed to be minimised to allow for an electrical trim this results in a large PCR value. From the PCR, a VCR value can be derived based solely on self heating. The VCR shows a nonlinearity of 150 ppm or 0.015 % over the resistors voltage range. This is acceptable for the X452B but needs to be improved on if the trim method is to further refined. The speed of the trim was restricted in the present setup, but the proposed new test method from Figure 5-18 reduces trim time and leads to improved cost efficiency. This allows for greater availability of the technology in a commercial product.

The proven robustness of the technology allows for the integration of the iTrim resistors in many applications where the device experiences extreme temperatures and harsh environments. The sum of the high precision absolute resistance, low TCR, high reliability and low cost together combine to make the trim a successful technique.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absolute Resistance</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>Absolute tolerance post trim</td>
<td>0.02 %</td>
</tr>
<tr>
<td>Absolute TCR</td>
<td>3 ppm/°C</td>
</tr>
<tr>
<td>PCR</td>
<td>60,000 ppm/W</td>
</tr>
<tr>
<td>VCR (Based from PCR)</td>
<td>30 ppm/V</td>
</tr>
<tr>
<td>Voltage Rating</td>
<td>5 V</td>
</tr>
<tr>
<td>Current Rating</td>
<td>0.5 mA</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-45 °C to 125 °C</td>
</tr>
<tr>
<td>Lifetime @ 55 °C</td>
<td>10,000 hours</td>
</tr>
<tr>
<td>Lifetime Drift</td>
<td>0.07 %</td>
</tr>
<tr>
<td>Test trim time</td>
<td>2.5 s</td>
</tr>
</tbody>
</table>

Table 5-2: X452B post trim specifications.
Chapter 5: X452B 10 kΩ Resistor Characterisation and Trim

5.8. Bibliography


6. Conclusion and Future Work

This thesis presented the successful modification of the TCR and absolute resistance, of an integrated resistor using an electrical trim. \textit{iTrim}'s novelty was not only in the successful trim of TCR and resistance but also in the characterisation method of the TCR and resistance values during the trim at a single ambient temperature. The combination of the trim accuracy and efficient trim method allows for a commercially viable technology that can be integrated into an IC. Although there are discrete resistors available that meet and exceed the performance of the post electrically trimmed SiCr resistor, these technologies consume area, reduce reliability through complexity of the PCB, and limit use through cost restrictions. \textit{iTrim} reduces the cost of achieving the target performance and eliminates the need for system manufacturers to specify and design in a precision discrete resistor onto the PCB. This task can be handled by the IC designer who best understands the requirements of the IC. The IC designer also benefits as there are reduced robustness circuitry requirements, which protect the IC from misapplication of the pins that are used to connect in a discrete resistor. These reasons support the progression of the \textit{iTrim} method from a research project to commercial use.
6.1. Thesis review

The Thesis opened with an overview of the various options for discrete and integrated precision resistors. It was clear from Tables 1-1 and 1-2 that the performance of commercially available integrated resistors were inferior to that of discrete solutions. Although the resistor film materials of discrete and integrated resistors were similar, the discrete resistors achieved this higher performance by depositing the resistive film on a purpose built substrate [1]. The discrete substrates were capable of physically changing with temperature to allow for some compensation of the TCR of the resistive film. As integrated resistive films need to be deposited on standard IC substrates, such as SiO₂, there were limited possibilities in adapting the substrate to improve the performance of the resistor. iTrim’s goal was to improve the integrated resistors TCR and absolute value by electrically trimming a SiCr resistor.

SiCr resistors are the best performing integrated resistors available to analogue IC design engineers. These resistors are available to the majority of analogue IC companies such as Analog Devices, Texas Instruments [2] and STMicroelectronics [3]. SiCr resistors are used in precision IC’s such as DACs, op-amps, potentiometers and voltage references. Integrated SiCr resistors have a good post fabrication TCR of typically -25 ppm/°C and a post LASER trim absolute resistance accuracy of 0.01 %. iTrim was developed to reduce the TCR further and allow for a post assembly trim. iTrim accomplished this by applying an electrical pulse to heat the film. Although electrically trimming the SiCr resistor has been attempted before, there were limits in the accuracy of the trim. This was because it is not commercially viable to perform a number of ambient temperature sweeps to accurately characterise the TCR during the trimming process. Instead previous attempts of TCR trim were based on characterisation data that guided the trim close to the target. To achieve a higher accuracy, iTrim used the PCR of the SiCr resistor to characterise the TCR of the resistor during the trim process.

To evaluate the relationship between the PCR and TCR of the SiCr resistor a test setup was developed. The test system was based on a LTZ1000ACH voltage reference [4] and AD5791, 20 bit DAC [5], which were used as a precision power supply with a voltage range of 20V. The resistance measurement was performed using a 34970A switch.
system and a 3458A multimeter [6]. The test system was capable of measuring the resistance to accuracies of 15 ppm and across a temperature range of -50 °C to 150 °C. Using this characterisation test system, electrical and thermal performance data was gathered on a large number of SiCr resistors. These SiCr resistors test units had an array of widths and lengths which allowed for the understanding of the effects of the geometry of the resistor. It was discovered that the shorter the resistor the greater the random and systematic variation in resistor value and TCR. This was found to be related to an over etch of the TiW contacts. A thermal model was developed which used the thermal and electrical data to calculate the thermal conductivity of the material that surrounds the SiCr resistor. This resulted in Equation 3-31, which directly related the PCR of the SiCr resistor to the TCR of the resistor. Using the PCR as a reference, it was found that the TCR could be predicted with accuracies of less than 1 ppm/°C.

The same characterisation test system was then used to capture the change in TCR and resistance during the electrical trim. Through the generated data, a greater understanding of the electrical trim process was gained. It was discovered that the processes behind the trim included both thermal migration and electrical migration. By carrying out a TEM analysis on post trim resistors, it was found that these migration processes resulted in some Silicon from the centre of the film moving to underneath the TiW contacts. This resulted in a Silicon depleted and Chromium rich area in the centre of the resistor which increased the TCR and reduced the resistance. By controlling the amplitude of the trim pulse the migration process could be managed. This allowed for the possibility of using the electrical trim pulse as a trimming method.

From the data gathered, an ADICE model was developed to replicate the performance of the SiCr resistor under various electrical and thermal biases. Using the improved ADICE model a 10 kΩ resistor was designed that allowed for both the TCR and absolute resistance of the SiCr resistor to be trimmed post assembly. The 10 kΩ resistor comprised of a string of SiCr fuses and four iTrim resistors. The SiCr fuses were used to reduce the variation of the post fabricated resistor from +/- 6% to 0.6%. This reduced variation allowed for the use of the iTrim resistors to fine trim the absolute resistance and TCR. Using ADICE, a simulation showed the capability of trimming the 10 kΩ resistor to 3 ppm/°C and 0.01% absolute resistance tolerance.
The X452B test chip, with integrated 10 kΩ \(iTrim\) resistor, was evaluated using a bench top test setup. This bench top setup incorporated the precision power supply and 3458A multi meter previously used in the initial characterisation test setup. A PCB with a TSSOP socket was constructed with interface pins to an Aardvark SPI host adapter. Control of the X457 was achieved by controlling the Aardvark through a Labview vi. This test setup was first used to characterise the relationship between TCR and PCR plus the relationship between change in absolute resistance and PCR. A program was written that incorporated equations representing the fits of these relationships, to allow for the prediction of the required resistance trim of the four \(iTrim\) resistors that result in the target TCR and absolute resistance values. It was found that when using these predictions, the 10 kΩ integrated resistor could be trimmed to less than 3 ppm/°C and to an accuracy of 0.02%. This proved the concept of trimming both the absolute resistance and TCR post assembly to accuracies matching discrete solutions.

To confirm the robustness of the post trim 10 kΩ resistor a number of reliability tests were performed. The goals of the reliability test were to calculate the drift in absolute resistance for the stress tests. During the initial HTOL tests [7] the absolute resistance was found to drift by up to 0.07%. This was very high so to reduce the drift a post trim electrical pulse was applied to the \(iTrim\) resistor. This electrical pulse had a lower amplitude than the pulse used for trim but was high enough to anneal the film. This reduced the drift during HTOL to below 0.04%. Preconditioning tests [8] followed which also showed a drift of 0.04%. When HTOL was performed on these post precondition units, the drift between preconditioning and HTOL was only 0.01%. This proved that the thermal stresses of preconditioning match that of HTOL so the combined drift of these processes was 0.05%. Once drift from temperature cycling [9] and HAST tests [10] were include the total lifetime drift of the resistor was specified as 0.07% of the original absolute resistance value.

The overall post trim resistor specifications as detailed in Table 5-2, are impressive for an integrated resistor. The X452B demonstrates the successful application of \(iTrim\) to trim the TCR and absolute resistance for the integrated resistor. In the future work section proposed improvements of these specifications will be detailed.
Chapter 6: Conclusion and Future Work

6.2. Conclusion

The \textit{iTrim} method has successfully demonstrated the post assembly trim of the TCR and absolute resistance of an integrated precision resistor. This thesis has presented an overview of the research carried out to characterise the pre trim and post trim resistor. The research has resulted in the capability to accurately simulate the SiCr resistor and closely replicate the \textit{iTrim} trim routine in an ADICE environment. The capability to simulate the resistor allows for the design of an integrated resistor based on performance specifications of a particular IC. This thesis has shown that not only can the \textit{iTrim} method achieve high accuracies but it can also carry out the trim in a cost effective manner while minimising any effect on the reliability of the post trim resistor. All these factors show the project has met the goal of improving the electrical and thermal performance of integrated resistors towards equalling the performance of discrete resistors.

6.3. Future work

The main performance limitations of the 10 kΩ \textit{iTrim} resistor are the minimum TCR of 3 ppm/°C and the high PCR value of 60,000 ppm/W. This high PCR introduces a non-linearity into the resistors performance. The TCR is limited by the bow found in the resistance versus temperature plots of Figure 5-23. The bow is related to the non-linearity of the TCR and the mismatch of the initial negative TCR material with the newly created positive TCR materials. It is found that if the initial TCR is lower, the bow is spread over a larger temperature range reducing the post trim TCR. One of the reasons behind the high TCR value is the use of 2 µm wide by 3 µm long \textit{iTrim} resistors. If the resistor used for electrical trim were made wider and longer, the sheet resistance would reduce as seen in Figure 3-14. This would also result in a lower TCR due to the sheet resistance and TCR relationship shown in Figure 3-19. The difficulty with increasing the width is the need for a higher current density to trim the resistor, while increasing the length means a greater voltage potential required for the trim.

The high PCR value is an issue when the max voltage potential across the resistor is close to the max voltage available for trim. This was the case with the X452B where the
Chapter 6: Conclusion and Future Work

max voltage for trim was 6 V while there would be a maximum of a 5V potential applied across the resistor in applications. From Table 5-2, the PCR is specified as 60,000 ppm/W. This can be converted to ppm/V as the resistor is a fixed 10 kΩ value. Over 5 V, the nonlinearity of the 10 kΩ resistor would be 150 ppm or 0.015%. This is quite large especially if the tolerance of the resistor is rated at 0.01%. There would be two approaches to reducing the PCR. The first is as detailed above, reducing the TCR of the 10 kΩ resistor. If the initial TCR was reduced by 50%, the final PCR should also reduce by 50%. To achieve this, the width and length of the iTrim resistors would need to increase. Another possibility is to isolate the iTrim resistors from the IC. The iTrim resistors would be connected to bond pads and then bonded to another bond pad on the IC to connect in the resistor. The advantage of isolating the iTrim resistor is that higher voltages can be used to trim the resistor using a probe station. The probe station could also short the iTrim resistors to the IC during characterisation to get an accurate measurement of the entire resistor string. The higher voltages would mean much larger resistors could be used which have lower TCR and PCR values. The disadvantage of this method would be the loss of post assembly trim capability and exposing the resistor to the mechanical stresses associated with assembling a die into a package. These stresses could result in significant drifts of absolute resistance.

Although the TCR and PCR are listed as the two main limitations of the iTrim resistors electrical and thermal performance, the current values would be tolerated in an IC design. The solutions to reducing the TCR and PCR listed above do not require significant technology development but rather there is a need for compromise to make sure that the required specifications are met. At the time of writing there is a project in progress to further refine the iTrim resistor.
Chapter 6: Conclusion and Future Work

6.4. Bibliography


Appendices

A. Thesis CD content

B. Table of reliability test units

C. Papers and patents associated with thesis
Appendices

Appendix A

The content of the attached CD are as follows:

- Thesis in pdf format
- Thesis Abstract in pdf and Microsoft Word format
- Labview 2011 folders. For use these files are to be loaded into the instr.lib folder.
  - “SiCr_resistor_eval” – Folder which contains vi files used to generate data in Chapter 3 and 4.
  - “X452B_eval” – Folder which contains vi files used to generate data in Chapter 5.
  - “Drivers” – Folder which contains National Instruments developed drivers and Analog Devices developed drivers for the AD5791, 34970A, 34401A and 3458A.
##Appendices

###Appendix B

Tables B-1 to B-3 below list trim and test conditions for units used to evaluate the reliability of the electrical trim method. Further details can be found in section 5.5 of Chapter 5.

<table>
<thead>
<tr>
<th>Test</th>
<th>Unit number</th>
<th>No. of trim resistors trimmed</th>
<th>Value of resistance trim (Ohm)</th>
<th>Total resistance trim amount (Ohm)</th>
<th>Anneal pulse duration (secs)</th>
<th>Fuses blown</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 hrs HTOL</td>
<td>4</td>
<td>4</td>
<td>-5</td>
<td>-20</td>
<td>0</td>
<td>No</td>
</tr>
<tr>
<td>500 hrs HTOL</td>
<td>5</td>
<td>4</td>
<td>-30</td>
<td>-120</td>
<td>0</td>
<td>No</td>
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<td>500 hrs HTOL</td>
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<td>4</td>
<td>-50</td>
<td>-200</td>
<td>0</td>
<td>No</td>
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<td>4</td>
<td>-60</td>
<td>-240</td>
<td>0</td>
<td>No</td>
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<td>-80</td>
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<td>No</td>
</tr>
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<td>-150</td>
<td>-600</td>
<td>0</td>
<td>No</td>
</tr>
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<td>-400</td>
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</tr>
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<td>500 hrs HTOL</td>
<td>18</td>
<td>4</td>
<td>-5</td>
<td>-20</td>
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<td>-800</td>
<td>5</td>
<td>No</td>
</tr>
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<td>500 hrs HTOL</td>
<td>25</td>
<td>4</td>
<td>-5</td>
<td>-20</td>
<td>2</td>
<td>Yes</td>
</tr>
<tr>
<td>500 hrs HTOL</td>
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<td>-120</td>
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<td>500 hrs HTOL</td>
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<td>-50</td>
<td>-200</td>
<td>2</td>
<td>Yes</td>
</tr>
<tr>
<td>500 hrs HTOL</td>
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<td>4</td>
<td>-60</td>
<td>-240</td>
<td>2</td>
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**Table B-1:** List of units in X452B1 reliability test.
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<th>Total resistance trim amount (Ohm)</th>
<th>Anneal pulse duration (secs)</th>
<th>Fuses blown</th>
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### Precondition MSL3 + 168 hrs HTOL

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<th>Total resistance trim amount (Ohm)</th>
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### Table B-2: List of units in X452B5 reliability test.

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### Table B-2: List of units in X452B7 reliability test.

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### Table B-2: List of units in X452B7 reliability test.
Appendices

Appendix C

Below are a list of papers and patents associated with the work detailed in this thesis

**Papers**


**Patents**

