An Isolated Power Factor Corrected Power Supply
Utilizing the Transformer Leakage Inductance

Thomas Conway

Abstract—The widespread use of electronic devices increases the need for compact power factor corrected power supplies. This paper describes an isolated power factor corrected power supply that utilizes the leakage inductance of the isolation transformer to provide boost inductor functionality. The bulk capacitor is in the isolated part of the power supply allowing for controlled startup without dedicated surge limiting components. A control method based on switch timing and input/output voltage measurements is developed to jointly achieve voltage regulation and input power factor control. A prototype design is implemented with detailed measurements and waveforms shown to confirm the desired functionality.

Index Terms—AC-DC Power Conversion, Power Factor Correction, Transformer Leakage Inductance.

I. INTRODUCTION

The widespread use of electronic devices from single phase AC supplies necessitates the increasing use of power factor corrected (PFC) power supplies in many applications including electronic equipment, computer servers and consumer products. PFC power supplies provide low total harmonic distortion (THD) in the current drawn from the line and this is an increasingly important requirement.

Power factor correction techniques have been researched widely in the literature [1][2] and active PFC using high frequency switching techniques [3] are now commonly used. The overarching principle involves controlling the input current drawn from the mains input to achieve the required current shape for low THD and high power factor. The power supply must provide a regulated DC output voltage and for many applications, galvanic isolation is also required.

The basic boost or step-up converter [4] forms the core of most architectures as it has an input inductor that allows input current control to be readily achieved. The well known flyback converter can be derived from the buck-boost converter, but with a transformer for output voltage isolation [4].

Traditionally for PFC supplies, flyback converters have been used for lower power levels (≤ 100W). For higher power levels (≥ 500W), a separate boost converter for PFC and separate DC to DC converter with transformer isolation for output DC voltage regulation is used.

A. Brief Review of Published Isolated PFC Converters

For lower power levels, flyback type architectures, often using a single switching element can provide PFC functionality, and use an output bulk capacitor for energy storage. A range of flyback based power factor corrected power supplies have been developed and are described in the literature. Ref. [5] describes a 60W flyback PFC supply to achieve IEC61000 THD requirements. A 10W to 30W LED lighting supply is described in [6] and another 60W supply described in [7]. A 72W flyback design is shown in [8] and a 100W flyback PFC design in described in [9]. In these architectures, the flyback transformer initially stores energy from the input source and then releases it to the output bulk capacitor. The transformer thus provides the PFC input current control and galvanic isolation. However, the need to store all the energy in the flyback transformer, the unidirectional core excitation [4], high voltage stresses in the switching device and difficulties with the transformer leakage inductance, limit the usage of such power supplies to lower power levels.

At higher power levels, two stage supplies with a separate boost PFC stage and isolated DC to DC stage are widespread. They typically consist of a power factor correction stage, based around a boost converter with large bulk storage capacitor to control the input line current, followed by an inverter driving a high frequency isolation transformer and finally an output stage with at least some filtering components. Such designs work well, especially when there is a need to supply a number of different voltage rails and a long holdup time is required. Most of these architectures use one (or more) boost inductors in the active PFC stage [3], and such inductors need to handle the full supply power levels resulting in a significantly sized component. The design of such front end PFC converters is a tradeoff between boost inductor size and high frequency losses [10]. Also, cascading multiple power stages leads to reduced overall efficiencies. The front end boost PFC stage typically has high in-rush current on startup, or needs additional components to limit the in-rush current [11][12].

Therefore, there has been considerable research published on other architectures that attempt to eliminate or mitigate some of the disadvantages of both the flyback and two stage PFC AC/DC power supplies.

A quasi-active PFC converter in [14] delivers 100W using a combined PFC cell with two transformers, one operating as a flyback converter and one operating as a forward converter. This allows parallel power transfer and avoids lossy snubber networks, all with a single controlled switch, but at the expense
of a number of magnetic cores and inductor elements.

A combination of a separate boost stage cascaded with a lossless snubber network is presented in [15], delivering 96W. Again only a single controlled switch is used but a number of separate magnetic cores and inductor elements are required.

For higher power levels, modified two stage structures have been proposed. An architecture to improve on the existing two stage PFC is described in [10] which moves the boost inductor and bulk capacitor to the isolated side of a resonant LLC converter with the effect of improving the voltage stresses on the switching devices and providing an output power of 250W.

A two stage structure proposed in [16] uses a boost converter PFC with a resonant LLC converter. The design uses transformer coupled power transfer from the boost inductor to the output. Using two transformers (one providing the boost inductor functionality), a power output of 480W is provided.

B. Proposed PFC Architecture

In this paper an active power factor corrected power supply is described, whereby the leakage inductance of the high frequency isolation transformer is used to provide the functionality of the boost inductor. Minimization of the leakage inductance in high frequency isolation transformers is normally desirable in most DC to DC converters, although resonant and soft switching architectures do use a controlled amount of leakage inductance [17] for the purpose of reducing switching losses.

The use of a controlled amount of leakage inductance is proposed in this paper to eliminate the need for two separate magnetic components in the two stage PFC converter and instead uses one magnetic component to achieve both the power factor correction and galvanic isolation.

In-rush current on startup can also be controlled by implementing a soft start strategy whereby the large bulk capacitor is initially charged up in a controlled manner.

Bidirectional core excitation is used, with part of the energy transferred via transformer action, and part stored in the transformer leakage inductance. The described architecture provides a useful technique at power levels above those suitable for single stage flyback type converters.

The technique lends itself to the adoption of wide bandgap semiconductor devices [18] with hard switching [19][20]. Typically applications might include LED lighting, electronic equipment, server power supplies and on-board chargers for electric vehicles.

In this paper, section II describes the proposed architecture. A simplified system model for the power electronics is outlined in section III, from which the basic operating modes of the circuit are identified and characterized. The dynamic selection of the operating modes and their control parameters to achieve power factor correction are presented in section IV. An example design for a 300W 50V power supply is shown in section V with an experimental prototype constructed, its operation confirmed, and waveforms and measurements presented in section V-B.
regulation is achieved by controlling the ratio of instantaneous current drawn to the instantaneous voltage applied and this control functionality operates at a slow rate comparable with the input source frequency, denoted $f_{AC}$.

In effect, the transformer leakage inductance and secondary shorting switch act as a step up or boost converter with the output rectifier and bulk capacitor $C_B$. However, the input voltage polarity reverses once each cycle and the boost operation is carried out in two $T/2$ time periods, each with opposite polarity voltage and current waveforms.

III. THEORY OF OPERATION

Fig. 4 shows a simplified circuit model for the proposed power supply. Assuming the switching frequency of the converter is very high compared to the AC source frequency, the input to the transformer can be considered to be essentially a 50% duty cycle square wave with period $T$ and peak amplitude $\pm V_I$. The model in Fig. 4 is referenced to the secondary side of the transformer and the voltage amplitude into the transformer model is the primary voltage $V_P(t)$ multiplied by the turns ratio of the transformer, or

$$V_I[kT] = \left| V_P(kT) \frac{N_s}{N_p} \right|$$

(1)

Fig. 2. Qualitative voltage waveforms for the circuit of Fig. 1 over a full AC cycle.

Fig. 3. Qualitative current waveforms for the circuit of Fig. 1 over a full AC cycle.

Fig. 4. Circuit diagram of the proposed power supply architecture.

The operation of the circuit is based on the assumption that the transformer magnetizing inductance $L_M$ has little effect on the operation of the circuit other than to add a magnetizing current to the input source. Simulations show that magnetizing currents significantly less (a factor of $\frac{1}{5}$ or less), than the currents being transferred, have little impact on the circuit overall functionality. This is verified in the experimental prototype waveforms of section V-B.

The total leakage inductance of the transformer is denoted $L_L$ and the current flowing out of the transformer secondary winding is denoted $I_L(t)$.

The operation of the system is essentially that of a step up or boost converter and is based around the timing of shorting switch $S_1$ in Fig. 4. At the beginning of a switching cycle, the input voltage switches to $+V_I$ (dropping the $[kT]$ for notation for clarity) and simultaneously the shorting switch $S_1$ is turned on. The current $I_L(t)$ in the leakage inductance $L_L$ rises linearly while the switch $S_1$ is on. When the switch $S_1$ is turned off, the current in the leakage inductance is forced through the rectifier diode bridge formed by $D_1$, $D_2$, $D_3$, and $D_4$, and into the capacitor $C_B$ and system load, and the current in the leakage inductance falls. After a period of $\frac{T}{2}$,
the input voltage changes sign to $-V_I$ and the same operation occurs, except for a change in the sign of the inductor current. Two distinct operation modes of the circuit can be identified depending on whether the leakage inductance current starts at zero and returns to zero before time $T/2$, denoted as the discontinuous conduction mode (DCM), or when the leakage inductance current starts the cycle with a non-zero (negative) value, retains a non-zero (positive) value at time $T/2$ and returns to a non-zero (negative) value at the end of the cycle (time $T$), denoted as the continuous conduction mode (CCM).

To achieve unity power factor, the circuit needs to be operated in such a manner as to control the input current drawn from the supply. The two operating modes are now discussed in detail to relate the input current drawn to the timing period $T_1$.

**A. Discontinuous Conduction Mode (DCM)**

Fig. 5(a) shows the input voltage $V_i(t)$, the secondary voltage $V_S(t)$, the leakage inductor current $I_L(t)$ and the current into and out of the output rectifier $I_X(t)$ and $I_Y(t)$ as well as the switch current $I_{S1}(t)$, for the circuit operating in discontinuous conduction mode. With the shorting switch $S_1$ closed, the leakage inductor current $I_L(t)$ rises from zero to the value $+I_P$ over the set period $T_1$, thus:

$$I_P = V_1T_1/L_L$$

(2)

When the shorting switch $S_1$ opens, the inductor current falls back to zero over a period $T_2$ with the relationship:

$$I_P = (V_O - V_1)T_2/L_L$$

(3)

The sum of the periods must be less than the half period $T/2$ to ensure operation in the discontinuous conduction mode or:

$$T_1 + T_2 \leq \frac{T}{2}$$

(4)

The average input current to the transformer model (ignoring the magnetizing inductance) over the period $T/2$ can then be calculated as:

$$I_L^* = \frac{1}{2}I_P\frac{T_1 + T_2}{T_2}$$

(5)

and combining with eqn. 2 and eqn. 3, the average input current is:

$$I_L^* = \frac{T_1^2}{T L_L} \left( \frac{V_1 V_O}{V_O - V_1} \right)$$

(6)

The actual input current from the AC source is a scaled version of this current and is:

$$I_M = \frac{1}{2} N_s N_p I_L^*$$

(7)

with any contribution from the magnetizing inductance averaging to zero over each $T$ period.

It is apparent by considering eqn. 1 and eqn. 7, that achieving unity power factor in the input source is equivalent to controlling the current value $I_L^*$ to be directly proportional to $V_I$. Denoting the constant of proportionality as $G_M$, or $I_L^* = G_M V_I$, then substituting in eqn. 6 and rearranging yields the equation:

$$T_1 = \frac{G_M T L_L (V_O - V_1)}{V_O}$$

(8)

The equation shows that given a constant of proportionality as $G_M$, the required time period $T_1$ can be calculated by knowledge of the system parameters $L_L$ and $T$, measurement of the output voltage $V_O$ and calculating $V_I$ by measurement of the rectified input source voltage and scaling by a factor of $1/2N_p$.

**B. Continuous Conduction Mode (CCM)**

Fig. 5(b) shows the input voltage $V_i(t)$, the secondary voltage $V_S(t)$, the leakage inductor current $I_L(t)$ and the current into and out of the output rectifier $I_X(t)$ and $I_Y(t)$ as well as the switch current $I_{S1}(t)$, for the circuit operating in continuous conduction mode. With the shorting switch $S_1$ closed, the leakage inductor current $I_L(t)$ rises from the value $-I_E$ to the value $+I_P$ over the set period $T_1$ thus:

$$I_P + I_E = V_1T_1/L_L$$

(9)

When the shorting switch $S_1$ opens, the inductor current falls back to $+I_E$ over a period $T_2 = T - T_1$ with the relationship:

$$I_P - I_E = (V_O - V_1)T_2/L_L$$

(10)

The average input current to the transformer model (ignoring the magnetizing inductance) over the period $T/2$ can then be calculated as:

$$I_L^* = \frac{1}{2}(I_P - I_E)T_1 + \frac{1}{2}(I_P + I_E)T_2$$

(11)

and combining with eqn. 9 and eqn. 10, the average input current can be shown to be:

$$I_L^* = \left( \frac{1}{2} \right) T_1 T_2 - T_1^2 \frac{V_O}{T L_L}$$

(12)

With $I_L^* = G_M V_I$, then substituting in eqn. 12 and rearranging yields the equation:

$$T_1 = \frac{T}{4} \left( 1 - \sqrt{1 - \frac{16G_M L_L V_I}{T V_O}} \right)$$

(13)

Similar to section III-A, this equation shows that given a constant of proportionality $G_M$, the required time period $T_1$ can be calculated from $L_L$, $T$, $V_O$ and $V_I$. 
C. Power Handling Capability

The power capability of converter is determined by the maximum value of $G_M$ supported which is limited by the requirement for equation 13 to result in a real number. This requires the argument under the square root to be non-negative and hence

$$\frac{16G_{M\text{max}}L_LV_I}{T_{VO}} \leq 1$$

and with a maximum input voltage $V_{I\text{max}} = \sqrt{2}V_{AC}\frac{N_N}{N_p}$, yields a power capability $P_{\text{max}} = \frac{1}{2}G_{M\text{max}}V_{I\text{max}}^2$ of:

$$P_{\text{max}} \leq \frac{V_{AC}\frac{N_N}{N_p}V_O}{32\sqrt{2}f_sL_L}$$  \hspace{1cm} (14)

This equation can be used as a basis for converter design as demonstrated by the prototype example in section V. The maximum peak current in the leakage inductor during the CCM can be calculated as:

$$I_{P\text{max}} = \frac{V_{OT}}{8L_L}$$  \hspace{1cm} (15)

and the transformer must be designed to handle this peak current without saturation.

IV. Power Supply Control

The control objective for the power supply is to provide a constant output voltage and unity input power factor. This requires measurement of the output voltage and adjustment of the input current through the $G_M$ factor defined in section III-A. However, calculating the time parameter $T_1$ in section III-A and III-B also requires knowledge of the parameter $L_L$, the leakage inductance, which may not be accurately known. Therefore a new control parameter $K$ is defined as:

$$K = \frac{G_ML_L}{T}$$  \hspace{1cm} (16)

and $K$ is used for control rather than $G_M$. Substituting into eqn. 8 and eqn. 13 results in the required calculations for DCM as:

$$T_1 = T\sqrt{K\left(\frac{V_O - V_I}{V_O}\right)}$$  \hspace{1cm} (17)

and CCM as:

$$T_1 = \frac{T}{4}\left(1 - \sqrt{1 - \frac{16KV_I}{V_O}}\right)$$  \hspace{1cm} (18)
It can further be shown that the boundary condition of eqn. 4 can be written as:

\[ V_O(1 - 4K) \geq V_I \]  (19)

The feedback loop of Fig. 6 can then be used to control the power supply. In Fig. 6, the power supply output voltage \( V_O \) is measured and compared to a reference voltage \( V_{REF} \) to produce an output voltage error \( V_{ERR} = V_O - V_{REF} \). This error voltage is used by a PID controller with dynamics below the input AC frequency \( f_{AC} \) to adjust the variable \( K \) to control the output voltage \( V_O \).

The variable \( K \), is used in the timing generator to generate the inverter timing and the secondary shorting period \( T_1 \) twice per sample period \( T \). The timing generator uses the measured power supply output voltage \( V_O \), and a scaled version of the input rectifier voltage \( V_R \) as \( V_I = \frac{1}{2} N_s N_p V_R \). Using \( K \), \( V_I \) and input voltage \( V_{AC} \) is based on selecting a desired switching frequency \( f_s \), calculating the maximum transformer turns ratio \( \frac{N_s}{N_p} \), and using eqn. 14 to determine the maximum allowed value of leakage inductance.

Consider the design of a 300W 50V power supply with a 240Vrms AC 50Hz source or \( P = 300W \), \( V_O = 50V \) and \( V_{AC} \leq 240Vrms \). A switching frequency of \( f_s = 50kHz \) is chosen for this example.

Operation in boost mode requires the peak transformer output voltage to be not greater than the desired output voltage and thus

\[ \frac{N_s}{N_p} \leq \frac{2V_O}{\sqrt{2}V_{AC}} \]

or \( \frac{N_s}{N_p} \leq 0.295 \). Choosing \( \frac{N_s}{N_p} = \frac{6}{32} \), then rearranging eqn. 14 to:

\[ L_L \leq \frac{V_{AC} N_s N_p V_O}{32\sqrt{2} f_s P} \]

imposes the requirement that \( L_L \leq 4.82\mu H \). With these parameters, the maximum transformer peak current can be calculated from eqn. 15 as 26.0 A.

\[ \text{V. Example Prototype Design} \]

Design of a converter using the proposed technique for a given power level \( P \), an output voltage \( V_O \) and a maximum operating mode, the calculated shorting period reduces as the load level drops.

The calculations for shorting period \( T_1 \) need to be calculated in real-time by the controller at a rate considerably higher than the input frequency \( f_{AC} \), though not necessarily at the full \( f_s \) rate. Egn. 19, eqn. 17 and eqn. 18 can be readily implemented in a modern microcontroller, DSP or FPGA at the required data rates.

\[ \text{A. Transformer Design} \]

The transformer design for the prototype is based on using two E-Cores with the primary winding on one core and the secondary winding on the other core as in Fig. 8(a). This results in a transformer with good magnetizing inductance and a usable amount of leakage inductance. The transformer design requirements are to provide the specified leakage inductance and maximum magnetizing inductance, while preventing core saturation under peak operating currents. Fig. 8(b) shows a magnetic reluctance model for the transformer with the leakage being modeled by the air gap reluctance \( R_g \) between the central core and the outer legs. The central core reluctance is \( R_C \) and the reluctance of each top and side halves is \( R_O \).
The final reluctance model, Fig. 8(c) can then be used with the equations:

\[
\mathcal{R}_M = 2\mathcal{R}_C + \mathcal{R}_O + 2\left(\frac{\mathcal{R}_C + \frac{\mathcal{R}_O}{\mathcal{R}_g}}{2}\right)^2,
\]

\[
\mathcal{R}_K = \mathcal{R}_C + \frac{\mathcal{R}_O}{2} + \mathcal{R}_g.
\]

The resulting magnetizing inductance (from the primary side) is \( L_P = \frac{N_P^2}{\mathcal{R}_M} \) and total leakage inductance (from the secondary side) is \( L_L = 2\frac{N_S^2}{\mathcal{R}_K} \).

The peak core magnetic flux \( \Phi_{MAX} \) is then the sum of the magnetizing flux \( \frac{N_P I_M}{\mathcal{R}_M} \) and the leakage flux \( \frac{I_{PS} N_S}{\mathcal{R}_K} \), with \( I_M \) being the peak primary magnetizing current and \( I_{PS} \) being the peak secondary current. The peak core magnetic flux density with a core effective area of \( A_e \) then is:

\[
B_{MAX} = \frac{N_P I_M}{\mathcal{R}_M A_e} + \frac{I_{PS} N_S}{\mathcal{R}_K A_e}
\]  

(20)

![Fig. 8. Ecore transformer construction with flux paths for the leakage (solid) and magnetizing (dashed) inductances and corresponding magnetic models.](image)

The prototype transformer consists of a pair of E42/21/15 cores, 3C90 ferrite material, with 22 turns on the primary and 6 turns on the secondary. The corresponding magnetizing inductance (from the primary side) and total leakage inductance (from the secondary side) is calculated as:

\[
L_M = 1800\mu H \quad \text{and} \quad L_L = 4.7\mu H
\]

and the actual measured values are listed in Table I. With a 240\( V_{rms} \) AC input, the magnetizing current is \( \approx \pm 0.47A \) and with a peak secondary current of 26A, the peak core magnetic flux density based on equation 20 is

\[
B_{MAX} = 0.211T + 0.0562T \approx 0.27T.
\]

This value is less than the saturation magnetic flux density of 0.32\( T \), and only occurs at the peak of the input AC waveform. Notice that the contribution from the leakage flux is small due to the high reluctance of the leakage flux path as it passes through the air gap. This example shows that the addition of the leakage inductance does not severely impact on the size of transformer in terms of core saturation.

### B. Prototype Construction and Measurements

The power electronics schematic of the prototype power supply is shown in Fig. 9. A bridge rectifier \( B_{R1} \) is used to rectify the input AC voltage and a half bridge inverter based on MOSFETs M1 and M2 drive the transformer. The prototype is based on a semi synchronous rectifier for the output rectifier [21]. In this case, two MOSFETs M3 and M4 are used to perform the secondary shorting during the \( T_1 \) period by turning on both transistors. During the remaining time, only one of the transistors is left switched on to perform the rectification function in conjunction with one of the Schottky diodes, D1 or D2.

The measured parameters of the constructed prototype transformer are listed in Table I, together with the other power components used in the prototype power supply.

### Table I

**Prototype Component Values and Specification.**

<table>
<thead>
<tr>
<th>Component/Parameter</th>
<th>Specified/Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMC filter</td>
<td>3\times 100nF Capacitor</td>
</tr>
<tr>
<td>Bridge Rectifier B_{R1}</td>
<td>BU15065S-E3/45, 15A 600V Bridge Rectifier</td>
</tr>
<tr>
<td>MOSFETS M1, M2</td>
<td>1uF 250V Film Capacitor</td>
</tr>
<tr>
<td>Transformer</td>
<td>2\times Ecore 42/21/15 3C90</td>
</tr>
<tr>
<td>Turns Ratio</td>
<td>22:6</td>
</tr>
<tr>
<td>Primary Inductance</td>
<td>2.0 mH</td>
</tr>
<tr>
<td>Secondary Inductance</td>
<td>150 uH</td>
</tr>
<tr>
<td>Secondary Leaking Inductance</td>
<td>4.0 uH</td>
</tr>
<tr>
<td>Diodes D1, D2</td>
<td>MBR4060 60V 40A</td>
</tr>
<tr>
<td>MOSFETS M3, M4</td>
<td>IRFB4110 100V 120A</td>
</tr>
<tr>
<td>Bulk Capacitor</td>
<td>6000uF (6\times1000uF) 63V</td>
</tr>
<tr>
<td>Control Processor</td>
<td>LPC1114 ARM M0</td>
</tr>
</tbody>
</table>

Control of the prototype is implemented in firmware on a modern 32bit microcontroller. An internal 10 bit ADC measures the input rectified voltage and bulk capacitor output voltage. The microcontroller performs the calculations for the PID output voltage control and the timing calculations as per section IV with the timing signals generated with on-chip PWM generators.

Fig. 10 shows an image of the prototype power supply and its measured performance at 300W output power is given in Table II. Measured waveforms of the line input voltage and current and transformer primary voltage and current are shown in Fig. 11 over a full line cycle. Zoomed in waveforms of the transformer primary voltage and current and secondary voltage and current are shown in Fig. 12 (DCM) and Fig. 13 (CCM) and confirm the desired operation. The effect of finite values of bus capacitors C1 and C2 can be seen in the primary voltage waveform of Fig. 13 as a droop in the voltage rather than an ideal square wave.

The measured efficiency, power factor and total harmonic distortion are plotted against output power in Fig. 14. The
efficiency of the converter is determined by the component losses and an analytical model of the relative contributions results in the distribution shown in Fig. 15. The largest contributions are given by the Schottky diodes conduction losses and the transformer core and winding losses. Fig. 16 shows an infra red thermal image of the prototype showing the highest spot temperature on the windings of the transformer. Switching losses dominate in the secondary MOSFET switches and the use of faster switches such as GAN devices or soft switching techniques might be useful here particularly if a higher frequency of operation is adopted.

The prototype design is based on a fixed line input voltage and a fixed switching frequency of 50kHz. Further work could involve extending the architecture to operate as an universal supply over wide input voltage operation. While the existing design will work at lower input voltages, the output power is limited by the fixed switching frequency and leakage inductance value as per equation 14. For a given
TABLE II
MEASURED PERFORMANCE FOR THE EXPERIMENTAL PROTOTYPE.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>237.1 Vrms</td>
</tr>
<tr>
<td>Input Current</td>
<td>1.375 Arms</td>
</tr>
<tr>
<td>Input Power</td>
<td>320 W</td>
</tr>
<tr>
<td>Power Factor</td>
<td>0.98</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>49.8 V</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>3.8 V&lt;sub&gt;pp&lt;/sub&gt; (i.e. ±3.8%)</td>
</tr>
<tr>
<td>Output Current</td>
<td>6.02 A</td>
</tr>
<tr>
<td>Output Power</td>
<td>300 W</td>
</tr>
<tr>
<td>Efficiency</td>
<td>93.7%</td>
</tr>
<tr>
<td>THD</td>
<td>4.1%</td>
</tr>
</tbody>
</table>

power level, universal input voltage support could be addressed by adopting variable frequency operation with lower input voltages supported by reducing the switching frequency.

C. Comparison with existing designs

A key motivation for the work reported in this paper is the reduction of size and weight of the converter with a key component of these being the magnetic elements. Table III provides a comparison of the prototype developed with a range of PFC isolated supplies described in the literature. Flyback type architectures dominate at lower power levels (below 100W) with two stage architectures accounting for higher power levels. The prototype based on the proposed architecture in this paper compares well with the other designs and industry expectations [22], and should provide a useful topology for PFC converter designers.

VI. CONCLUSIONS

This paper describes an isolated AC/DC power supply using the leakage inductance of the isolation transformer to achieve active power factor correction. The proposed architecture allows for a compact lightweight power supply for power levels above that of flyback type PFC supplies. The principle of operation with two conduction modes is described and a timing based control method is developed for the power factor control. A prototype power supply is designed and constructed to verify experimentally the operating principle. Measurements confirm the active power factor correction functionality with high power factor and low THD.

The proposed power supply architecture is scalable and it should be feasible to extend the power capability of the proposed circuit to 500W or more. Further variations on the principle can be adopted such as universal input voltage operation, full bridge input inverter, zero current switching, synchronous rectification, interleaved designs and so forth. The proposed architecture provides an additional option for the designers of PFC isolated supplies.

REFERENCES

### Table III: Comparison with Other Isolated PFC Topologies.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Topology</th>
<th>Switching Frequency</th>
<th>Peak Power</th>
<th>Universal Voltage</th>
<th>Weight of Cores</th>
<th>Switches (S)</th>
<th>Diodes (D)</th>
<th>Efficiency</th>
<th>Power per Core Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>Flyback</td>
<td>65kHz</td>
<td>60W</td>
<td>Yes</td>
<td>31g</td>
<td>1 S, 5 D</td>
<td></td>
<td>89.5%</td>
<td>1.94 W/g</td>
</tr>
<tr>
<td>[7]</td>
<td>Flyback</td>
<td>(≥ 44kHz)</td>
<td>60W</td>
<td>Yes</td>
<td>36g</td>
<td>1 S, 5 D</td>
<td></td>
<td>91%</td>
<td>1.67 W/g</td>
</tr>
<tr>
<td>[8]</td>
<td>Flyback</td>
<td>40kHz</td>
<td>72W</td>
<td>No</td>
<td>36g</td>
<td>2 S, 2 D</td>
<td></td>
<td>90%</td>
<td>2.00 W/g</td>
</tr>
<tr>
<td>[15]</td>
<td>Boost-Flyback</td>
<td>50kHz</td>
<td>96W</td>
<td>Yes</td>
<td>120g</td>
<td>1 S, 7 D</td>
<td></td>
<td>90.6%</td>
<td>0.80 W/g</td>
</tr>
<tr>
<td>[14]</td>
<td>Quasi-Active Flyback</td>
<td>75kHz</td>
<td>100W</td>
<td>Yes</td>
<td>57g</td>
<td>1 S, 10 D</td>
<td></td>
<td>93%</td>
<td>1.75 W/g</td>
</tr>
<tr>
<td>[10]</td>
<td>Resonant LLC/Boost</td>
<td>90-450kHz</td>
<td>250W</td>
<td>Yes</td>
<td>92g</td>
<td>8 S, 4 D</td>
<td></td>
<td>94.5%</td>
<td>2.72 W/g</td>
</tr>
<tr>
<td>[16]</td>
<td>Boost/Resonant LLC</td>
<td>100kHz</td>
<td>480W</td>
<td>No</td>
<td>122g</td>
<td>5 S, 4 D</td>
<td></td>
<td>93.58%</td>
<td>3.93 W/g</td>
</tr>
<tr>
<td></td>
<td>This work</td>
<td>50kHz</td>
<td>300W</td>
<td>No</td>
<td>88g</td>
<td>4 S, 6 D</td>
<td></td>
<td>93.7%</td>
<td>3.41 W/g</td>
</tr>
</tbody>
</table>


Thomas Conway received the B.Eng. degree in electronic engineering and the Ph.D. degree in detection methods for magnetic recording channels from the University of Limerick, Ireland, in 1991 and 1996, respectively.

He joined Hewlett Packard CPB, Bristol, in 1991 and worked for two years on the design and development of tape drives for computer storage. From 1996 to 1998, he worked as a senior design engineer with Analog Devices B.V. Limerick, Ireland and Adaptec Inc., Longmont, CO, USA on disk drive read channels and controllers.

Since 1999, he has been a lecturer in the ECE Department, University of Limerick, Ireland and has lectured on VLSI and analogue IC design, information theory and coding, and more recently power electronics and electric vehicles.

Dr. Conway has worked as a design consultant for a number of Irish and international companies, and is also a researcher with CRIS - the Centre for Robotics & Intelligent Systems (www.cris.ul.ie) at the University of Limerick, Ireland.