Abstract

The trend in next-generation switched-mode power supplies will lead to modular, scalable solutions which can deliver power efficiently over a wide range of operation. Multiple parallel power stages, often called “phases”, are necessary to meet these requirements. This paper details a new approach to introduce more control features like phase-alignment, current sharing and phase shedding, which improve the efficiency of the overall dc-dc converter. An advantage of the proposed method is that it does not require communication signals between the individual controllers and is therefore fully scalable and cost effective. Experimental results for a FPGA prototype implementation are presented.

1 Introduction

Paralleling power supplies is a continuing trend in today’s power converter markets. For example, for high-current applications paralleling is required, due to the limitations in today’s semiconductor switches. Additional advantages like interleaving which emulates a higher switching frequency, contribute to this trend also.

Broadly speaking, there are three different system architectures deployed, depending on the application requirements:

1. Independent, parallel power supplies.
2. Multi-phase systems controlled by one central controller.
3. Multi-phase systems with one individual controller per phase communicating with each other via communication lines.

The first and simplest solution is a parallel connection of several independent power supplies. However, as the individual units are not “aware” of each other, more advanced control features like phase alignment, active current sharing or phase shedding cannot be utilized. Furthermore, the different power supplies can work “against” each other, leading to circulating currents between the power supplies or even beating in the output voltage, as the individual power supplies cannot differentiate between a current delivered from/to other phases and the actual load current.

A technique to avoid circulating currents is “droop current sharing” which uses the output impedance of the power supply, e.g. [1, 2], where the output voltage of each individual power supply is adjusted proportionally to its load current. With increasing load current, the power supply decreases its output voltage. As a consequence, other phases with lower load currents and therefore higher output voltages take more current. When the system reaches its equilibrium, each individual supply outputs equal output voltage and current, leading to an even current distribution. However, a droop current balancing scheme requires a load line/output impedance, which cannot be tolerated by most of today’s applications, leading to the necessity for alternative methods.

In order to address these drawbacks, active current sharing has gained a lot of research interest [3–8]. With a few exceptions, most of these schemes require the knowledge of the total output current at a central point. If the output power is required in a very dense area, “multi-phase power converters” can be used. This concept, illustrated in Fig. 1, uses several power stages in parallel controlled by one central power controller. The configuration is capable of supporting beneficial features, like phase shedding, current sharing and thermal regulation, as all required information is available to the controller. Conversely, the weakness in this configuration is the central control unit in terms of modularity and “hot-plugability”. To explain, the central control unit is mandatory during operation and cannot be replaced online.
Alternative approaches “split” the controller into one controller per phase (Fig. 2). Each controller regulates the output voltage on the common output voltage line and can adjust its output current using information obtained from the other controllers. Typically the output current is shared over a communication line. While this communication line can be easily implemented in analogue control using the intrinsic summation of current sources and defined output impedances on one common signal [3], its implementation has proven more difficult in the digital domain.

In [4], a so-called “chain-control” approach is presented. Each individual controller is part of a communication chain leading to a ring system distributing the current information. While this approach gives good transient and steady-state performance, it does not support hot-plugging and has limited fault tolerance, due to the required ring communication line. This also constrains the PCB design as the signal has to connect all individual phases in a chain.

In [9], an approach has been presented addressing the problem of phase alignment in scalable power supplies. A ring communication line connecting the individual phases in series is used to detect the total number of phases and align their switching action in the switching cycle. A LC estimation allows optimized sequencing to further reduce the ripple voltage. However, the approach does not utilize any current sharing or phase shedding techniques.

In this paper a novel approach to address the phase alignment and current sharing for independent parallel power supplies is presented. The approach does not require any communication lines between the individual phases, hence leading to very good scalability. With advanced features like phase alignment, current sharing and phase shedding, the system implements most of today’s techniques to improve the efficiency of switch mode power supplies.

2 System Level Design

The system design utilizes multiple independent power stages (phases) connected to the same input and output voltage (Fig. 3). Each individual phase is controlled by an independent digital core (Fig. 4). The control path consists of an ADC, a digital control law and a DPWM to generate the drive signal for the power stage. Additionally, the DPWM implements a feature to change the period (frequency) for single switching cycles controlled by
an external signal. This allows the phase alignment block to shift the phase of the power stage relative to the other constant phases. The phase detection block measures the phase alignment and generates the input signals for the phase alignment logic. The current sharing block implements the current sharing algorithm detailed in the following section. The complete system can be easily implemented in today’s digital processes and integrated into any existing control solution.

### 2.1 Phase Alignment Algorithm

The novel phase alignment approach presented utilizes the only common signals between the converters, i.e. the input and output voltage. By using the noise generated on the input or output voltage, the system is able to detect the number of phases and their phase alignment. This method of detection is possible as every switching operation of the individual phases creates noise and ripple voltage on the connected input/output capacitors.

With reference to Fig. 3, the input voltage is AC coupled and the resulting ripple signal is compared with an adjustable threshold voltage. The result of this comparison is passed to the controller where it is assessed and analyzed. The phase detection block detects the characteristic patterns generated by the noise during switching. As a result, the number of clock cycles between the patterns can be measured and processed by the new phase alignment algorithm.

Without loss of generality, the phase alignment algorithm is shown in Fig. 5 for a dual phase system. The time differences from the previous and to the next switching operation are measured. For an optimal, uniform phase distribution these should be equal. If they are not equal, the phase alignment algorithm will correct them. This algorithm runs continuously in the background as an “on-the-fly” change of the phase alignment is required due to the use of phase shedding techniques.

One advantage of the proposed algorithm is its simplicity in implementation. With reference to Fig. 6, the required digital blocks comprise of a simple up/down counter, a controlling state machine and two digital comparators. The up/down counter counts up during the time period \( t_1 \) between the pulse on the digital input stream and the switching signal of the active phase. On the drive signal of the active phase, it changes the direction and counts down until the pulse from the next stage occurs in the data stream \( t_2 \). The two comparators assess the sign of the result with a dead band defined by the scalar \( \epsilon \). If the counter value is negative, meaning \( t_1 < t_2 \), the switching cycle is extended slightly during the next cycle. If the result is positive, the next switching cycle is shortened. If the value is inside the dead band proper phase alignment is assumed and no action is taken. This
2.2 Current Sharing

A different challenge for parallel power supplies is the sharing/balancing of the output power among the individual supplies. This is a necessary requirement: e.g. it prevents reverse current into the supplies. The efficiency can be improved by operating the phases at the optimal load currents.

Most of the existing solutions share the current equally among the phases and disable phases when the output power is below a predefined threshold – a technique called “phase shedding”. The disadvantage of this approach is that for distributed solutions it requires the sharing of the current information among the phases. Existing solutions use communication lines to provide this information (Fig. 2). Each phase regulates its current to a portion of the total output current dependent on the number of active phases. In multi-phase solutions, the central controller generally takes care of the current sharing itself.

The current sharing algorithm presented is based on optimal power levels (Fig. 7) instead of equal distribution over all available phases. This allows current sharing without the need of detailed current information from the individual phases where each controller adapts its output power by trying to operate at its optimal output power level. For an initial proof of concept, the optimal power levels are assumed to be zero (no load) and maximum load (Fig. 7). To elaborate, if the output power is below a defined threshold, the controller reduces its output power until it reaches zero. At this point, the phase in question will disable itself. Conversely, if the output power is high, the controller tries to increase the delivered output power to allow other phases to reduce theirs. If the output power is mid-range, each controller will decide independently to increase or decrease its output power if necessary.

A simplified version of the current transfer procedure is shown in Fig. 8. Prior to enabling the current sharing process, the system ensures that the output voltage and the inductor current are stable. The current sharing is then enabled after a random duration which is required to give other phases the opportunity to start their current transfer process. During the whole process, the output voltage is closely monitored. If the output voltage increases or decreases too much, the algorithm is disabled, because the output voltage regulation is of higher priority to the system.
One point to note is the small change of the output voltage during the current transfer between the individual power supplies. The size of the output voltage change is inversely proportional to the speed of the current transfer. If the voltage regulation is tight, the speed of the current transfer is limited.

3 Experimental Verification

The proposed algorithms have been implemented and verified on an Altera Cyclone II FPGA utilizing a DE2 board. The chosen power supplies are two buck converters with switching frequencies of 500 kHz each. For demonstration purposes, the two converters are implemented on the same PCB sharing the same FPGA. Two independent digital cores running in the FPGA are used to evaluate the final system configuration. The performance of the outlined phase alignment algorithm is shown in Fig. 9 and Fig. 10. The analogue signal shows the voltage at the pin of the comparator after AC filtering. Signals $D_1$ and $D_2$ show the drive signals for the high-side FETs where signal $D_{15}$ and $D_{14}$ show the data stream generated by the filter circuits and the data stream processed by the FPGA respectively. The delay between the comparator output signal and the data stream is due to the internal processing of the stream in the FPGA. It does not influence the proper operation of the system as it is internally compensated for. The phase alignment in Fig. 9 shows the alignment prior to the enabling of the alignment algorithm for an arbitrary initial phase shift. When the algorithm is enabled, the phases are aligned well (Fig. 10). The small offset from the perfect position is not relevant in practical applications. More importantly, the jitter of the phase alignment is very small, implying a stable result as a high jitter will lead to an undesirable oscillation of the phase alignment.

In Fig. 11, the two inductor currents are shown, together with the common output voltage (The visible solid “triangles” are caused by the limited resolution of the scope (aliasing effect)). The reaction of the current sharing algorithm is captured, where both supplies operate at approximately half their maximum power. One of the two phases takes the full current, while the second phase reduces its current to zero. It can then be disabled (phase shedding) which is not shown here. Also note that the output voltage changes slightly during the current transfer process, as it is required by the proposed system.

Figure 9: Phase alignment before enabling of the proposed alignment algorithm.

Figure 10: Phase alignment after enabling of the proposed alignment algorithm.

4 Conclusions

This paper presents a novel approach for digital control of independent parallel power converters and multi-phase dc-dc converters. This new method incorporates advanced features like phase alignment, active current sharing and phase dropping, and is thereby capable of increasing the efficiency of the total system significantly. The key advantage of the proposed approach over existing methods is that it can be implemented on distributed scalable systems without requiring any communication lines, i.e. additional “wiring”, between the controllers. The detailed digital system has been verified in experimental hardware.

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Figure 11: Experimental Verification of the Current Sharing Scheme.

References


