STATE-DEPENDENT ADC SCHEME FOR DIGITALLY ISOLATED SMPC

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ABSTRACT

This paper proposes a state-dependent Analog-to-Digital Conversion (ADC) scheme for digitally isolated Switched Mode Power Converters (SMPCs). The SMPC voltage range is subdivided into three different regions corresponding to the three different states the SMPC can be in: steady state and the two transient states "undershoot" and "overshoot". Each state uses a different, optimised ADC transfer function where the steady state region is sampled with higher resolution than the transient regions. This scheme reduces the number of bits to be transfered across the isolation barrier and therefore accommodates the use of data couplers with lower bandwidth or increased switching frequency.

Index Terms— ADC, state machine, digital, isolated, switched mode power converter

1. INTRODUCTION

In recent years a trend for digital control techniques of switched mode power supplies has emerged [1]. Digital control has a variety of advantages such as programmability, the use of adaptive control techniques and reduced sensitivity to external influences. However, it introduces the requirement for an analog-to-digital converter which provides a digital representation of the error voltage to the digital controller. The ADC resolution must be high enough to avoid negative quantisation effects [2].

For isolated power supplies additional considerations have to be taken into account, as it is required to tranmit the error signal across the isolation barrier. This channel can be either analog or digital. Some schemes are analogous to the classic analog controlled circuit shown in Fig. 1(a) and simply replace the analog controller and pulse width modulator (PWM) on the primary side, with an ADC, digital controller and a digital PWM (DPWM).

Alternatively the error voltage may be digitised on the secondary side and transmitted to the primary side using a digital coupler [3, 4] as shown in Fig. 1(b). This method removes any influence of coupler noise and aging on the control loop and therefore allows for more optimised controller parameters.

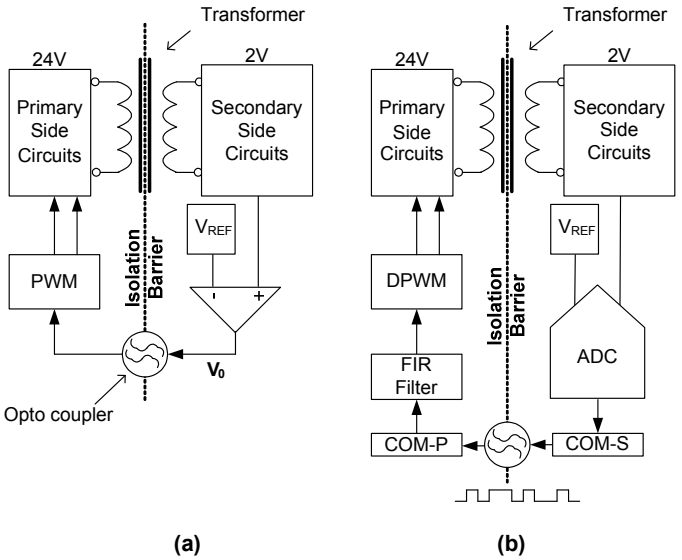

Fig. 1. (a) Analog Controlled Isolated SMPC. (b) Digitally Controlled Isolated SMPC.

The digital communication across the isolation barrier introduces a dependency between the ADC resolution (N_{adc}), the switching frequency (f_{sw}) and the coupler bandwidth, i.e. data rate. The digital coupler must be fast enough to transmit the full ADC value (digitised V_{err}) every switching cycle ($T_{\text{sw}} = 1/f_{\text{sw}}$) to allow the digital controller to take it into account for the next switching cycle. If this constraint is not met, an additional delay is introduced which has a large negative impact on the control loop.

In order to enable the use of high switching frequencies without the need for costly high-speed digital couplers, the number of bits representing the ADC value needs to be reduced. Standard data compression techniques are not suitable because they typically require larger data blocks, i.e. multiple ADC values. Simply reducing the ADC resolution would increase the quantisation effects and degrade the controller performance.

2. PROPOSED ADC SCHEME

This paper proposes a state-dependent ADC scheme for an isolated SMPC which reduces the number of bits required to be transmitted from secondary to primary side, while allowing a higher effective ADC resolution to be achieved.

2.1. Principle of Operation

The scheme subdivides the SMPC voltage range into three different regions corresponding to the three different states the SMPC can be in: steady state and the two transient states "undershoot" and "overshoot" (Fig. 2). For each state a different optimised ADC transfer function is applied (Fig. 3). In the steady state, the selected ADC transfer function has a fine resolution (N_{enc}-bit) in a voltage range around the nominal voltage. This voltage range is defined by the limits V_{low} and V_{high}. These are approximately $\pm 100\,\text{mV}$ in a typical SMPC. A fine resolution is necessary in this state to allow for stable loop behaviour. In the two transient states the corresponding ADC transfer functions map the same number of bits (N_{enc}-bit) to the appropriate voltage range below or above the steady state voltage range. Because these voltage ranges are larger the resulting resolution is now lower. This is sufficient during the transient states where fine control is not critical. The controller therefore needs to interpret the encoded ADC values in relation to the current state. The state machine shown in Fig. 4 is used to track the current state and to select the appropriate transfer function. The current state is changed whenever the last measured ADC value reaches either the minimum or maximum value.

2.2. Further Optimisations

The above basic setup has the drawback that during state changes the loop controller only receives the information that the value has left the current section and has to wait to receive

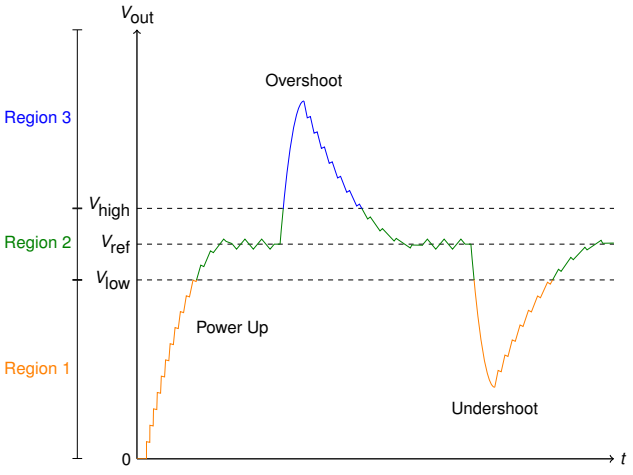

Fig. 2. SMPC operating regions.

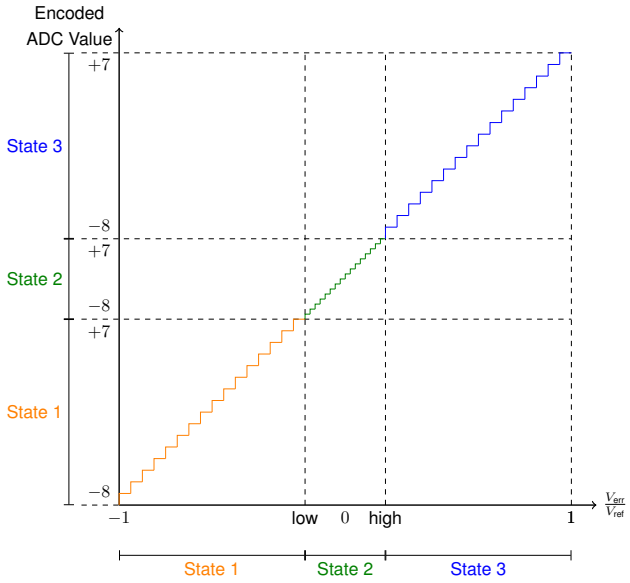

Fig. 3. State-Dependent ADC Transfer Function(s).

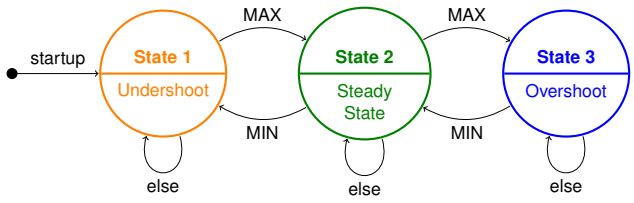

Fig. 4. ADC State Machine.

the next ADC value to obtain a more accurate value from the new transfer function. To minimise this non-linear behavior, the three transfer functions can also overlap. The steady state transfer function can additionally span each of the two transient operating regions with two coarse steps while still having fine steps inside the steady state voltage range. This allows the controller to immediately determine if the voltage has left the steady state by a large or small step. The next ADC value will be converted with the transient transfer function, providing a more accurate transient value. The transient transfer functions can in turn partially overlap with the steady state voltage range. This improves the controller accuracy when the value returns to the steady state operating region.

To avoid a noise peak triggering a state change, the ADC state machine can be extended to include two subsequent MAX or MIN values to change the encoding. This can be achieved using a 1-bit "counter" in the next-state logic or by including intermediate states between the three main states. These new states have the same output value, e.g. encoding, as the corresponding main states. If their entry condition (either MIN or MAX) remains fixed they proceed to the next state or otherwise return to the last state.

2.3. Implementation

The scheme can be implemented in two ways dependent on the chosen ADC architecture. If a standard linear full-range ADC (N_{adc}-bit) is used, its output value must be fed into an state-depending encoder. After transferring the encoded value (N_{enc}-bit) to the primary side a matching decoder maps it to a linear axis and provides it to the digital controller. This implementation is very favorable for rapid prototyping and testing. Fig. 5 shows the schematic of a SMPC circuit using this implementation. Alternatively an ADC can be designed with the state-dependent transfer function(s), making the encoder redundant. The fact that the power consumption of an ADC of this type is lower than that of a full-range ADC makes this implementation suitable for low power SMPC applications.

For this work an off-the-shelf 8-bit semi-flash ADC was used [5]. The value is encoded in the following way: In states 1 and 3 only the bits 6 to 3 are sent, while the MSB (7) is constant during one state and the three LSBs (2-0) are dropped. This results in the coarse steps shown in Fig. 3, except that one step overlaps with the corresponding side of the steady-state region as explained in section 2.2. During state 2 only the four LSBs are sent, giving the scheme the same fine resolution as 8-bit. The MSBs only hold the extended sign bit information in this case. The encoder must also watch for overrun conditions when the 8-bit value leaves the range of the current state and saturate the output value. In states 1 and 3 this is detectable by MSB alone. In state 2 the value is in range as long the bits 6-3 are identical and inverted to bit 7. Decoding back to 8-bit is done by substituting the dropped and implied bits accordantly.

The following code shows the Verilog implementation of both coders. (Note: The ADC provides an unsigned output value, where `8'b1000_0000` corresponds to $V_{\text{out}} = V_{\text{ref}}$, i.e. $V_{\text{err}} = 0$.)

Encoder

```
case (state):
  1: out[3:0] = in[7] ? 4'b0111 : {~in[6],in[5:3]};
  2: case (in[7:3]):
       5'b10000: out[3:0] = in[3:0];
       5'b01111: out[3:0] = in[3:0];
       default : out[3:0] = {~in[7],{3{in[7]}}};
     endcase
  3: out[3:0] = in[7] ? {~in[6],in[5:3]} : 4'b1000;
endcase
```

Decoder

```
case (state):
  1: out[7:0] = {1'b0,~in[3],in[2:0],3'b000};
  2: out[7:0] = {~in[3],{3{in[3]}},in[3:0]};
  3: out[7:0] = {1'b1,~in[3],in[2:0],3'b111};
endcase
```

3. EXPERIMENTAL VERIFICATION

The setup shown in Fig. 6, built from one custom SMPC board and two FPGA boards, was used to implement a digital controlled isolated SMPC with the proposed ADC scheme to verify the functionality and overall system stability. The implementation includes the intermediate states described in section 2.2. The error voltage is first digitised on the secondary side using the 8-bit ADC with $f_{\text{sample}} = f_{\text{sw}} = 250\,\text{kHz}$, $V_{\text{range}} = 0..4\,\text{V}$, $V_{\text{LSB}} = 15.6\,\text{mV}$. Its output word is fed to the secondary-side FPGA which applies the ADC encoding shown. The encoded V_{err} representation is then sent using to the primary-side FPGA using a digital coupler. The received data is decoded by the FPGA on the primary-side. This FPGA also implements the digital controller and the DPWM [6].

For comparison the load step response of the SMPC has been measured using full 8-bit, 4-bit and the proposed 4-

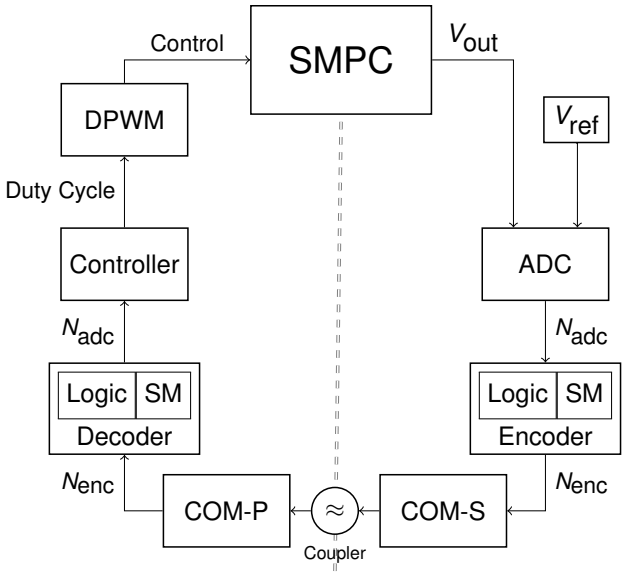

Fig. 5. SMPC with proposed ADC scheme.

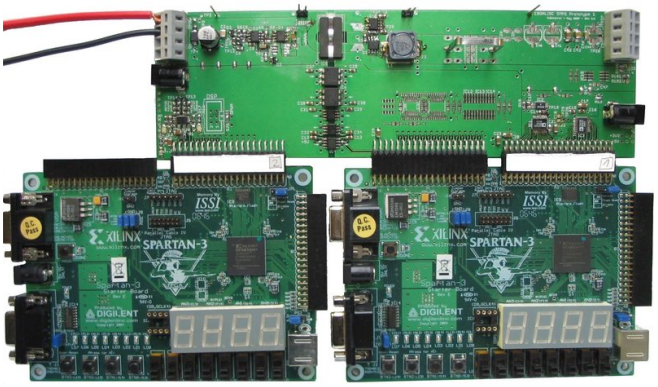

Fig. 6. Experimental Verification Platform. (top) SMPC board incl. dedicated ADC and data couplers. (bottom right) FPGA board implementing the encoder. (bottom left) FPGA board implementing the decoder, digital controller, DPWM.

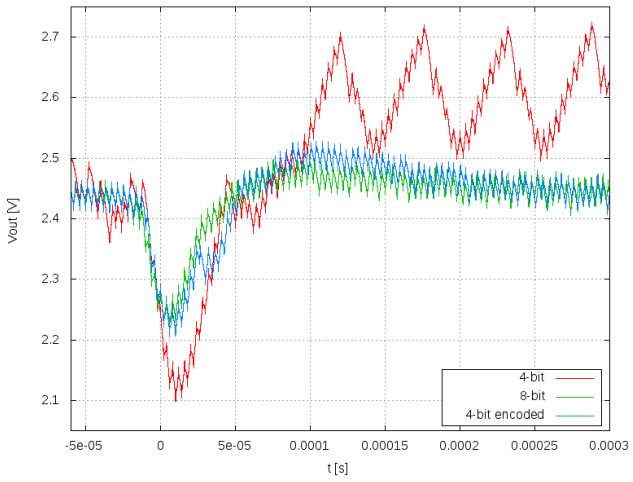

Fig. 7. Comparison of load step responses.

bit encoding resolution (Fig. 7). The 4-bit encoded scheme, while initially less precise, settles in a similar way as the full 8-bit ADC. Both show the same steady-state behaviour due to their identical fine resolution. In comparison, the non-encoded linear 4-bit ADC does not provide enough accuracy resulting in large limit cycling. The control law of the SMPC should hold the trailing overshoot caused by the load step undershoot inside the steady-state area of the ADC. This way an additional encoder state change is avoided which could prolong the step response.

In addition, Fig. 8 shows the power-up behaviour using the three different ADCs. While the lower accuracy of the encoded ADC in the overshoot area is clearly visible, the settling time to the nominal output voltage is comparable to the one of the 8-bit ADC. In contrast an unencoded 4-bit ADC shows a far less stable and precise settling behaviour.

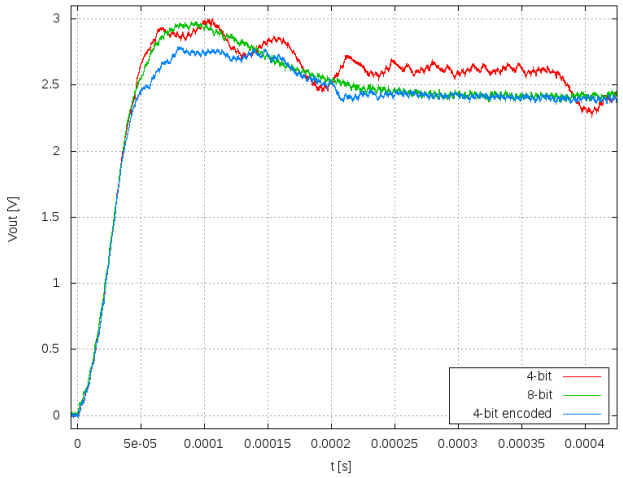

Fig. 8. Comparison of power-up behaviour.

4. CONCLUSION

A state dependent ADC scheme for SMPC has been proposed. It applies optimised ADC transfer functions to the steady and transient states. This allows for a fine resolution during the steady state while also covering a large transient area with sufficient resolution. In an isolated SMPC it reduces the number of bits to be transfered between the two isolated sides and therefore allows for higher switching frequencies without the need for faster data couplers. The scheme has been verified on a custom FPGA-based SMPC setup with $f_{\mathrm{sw}} = 250\,\mathrm{kHz}$ by encoding the output value of an dedicated 8-bit ADC.

The proposed scheme could be extended in different ways. To minimise the impact of the transition from fine to coarse resolution the state machine could be extended to five states where the two new states provide an intermediate resolution. The state-wise linear encodings can be adapted to be logarithmic and/or differential to further improve the effective resolution.

5. REFERENCES

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