Digitally Controlled Isolated SMPC with Bi-directional Data Transmission Scheme

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Abstract—This paper details the a digitally controlled isolated SMPC containing a novel bi-directional data transmission scheme. The bi-directional data transmission scheme avoids the effects of opto-coupler aging, allows the use of digital control techniques and enables transmission of auxiliary data from primary-to secondary and secondary-to primary. The complete digital controller was implemented on one custom and two FPGA boards, and achieves programmable regulation over the 0-2.5V range.

I. INTRODUCTION

Isolated power converters form an integral part of many power conversion systems [1, 2]. Analog control of an isolated Switched Mode Power Converters (SMPCs) supports the design of precise and inexpensive isolated SMPCs. Fig. 1(a). details an analog controlled isolated SMPC. The primary side high voltage DC or AC is converted to a low voltage DC signal across a transformer. The DC signal is compared with a reference level and an error signal $V_0$ generated. This error signal is transmitted to the primary side through an opto-coupler. The pulse width modulator (PWM) acts on this error signal generating signals that control switches on the primary side thereby regulating the secondary side voltage. Despite its low cost and simplicity it is recognized that the traditional analog controller suffers from a number of drawbacks:

- The LED of the opto-coupler suffers from a significant reduction of light emission over the life of the opto-coupler, particularly accelerated at high operating temperatures.
- Incompatibility with emerging digital SMPC control.
- High component count leading to reliability penalties, increased manufacturing cost, and material management challenges.
- Fixed output voltage (i.e. non-programmable), set through resistor network and voltage reference.
- Fixed frequency compensation, and closed-loop performance (set through passive networks), unsuitable for advanced, adaptive digital control
- In-ability to detect open-loop condition (missing or mal-functioning component in feedback path).

Fig. 1(b) details the digital control of an isolated SMPC. As in the analog case an error signal is generated on the secondary side but instead of an amplifier, an analog to digital converter is used to digitise the error signal. This error signal must be transmitted across the isolation barrier. The use of a digital transmission scheme has numerous advantages over the traditional analog approach. The effect of opto-coupler aging on the feedback signal is avoided [4]. Digital control techniques may also be utilised enabling programmability of control laws and output voltages. This paper presents a Bi-directional data transmission scheme for use in digitally controlled isolated SMPC. Section II details the key components of the digital controller incorporating the Bi-directional data transmission scheme. Section III details the implementation of the system on FPGA boards, Section IV details the performance of the system, finally section V presents a summary and conclusions.

![Fig. 1. (a) Analog Controlled Isolated SMPC. (b) Digitally Controlled Isolated SMPC.](image-url)
II. SYSTEM DESIGN

A. System Overview

The digitally controlled isolated SMPC is detailed in fig. 2. The system contains primary and secondary side SMPC circuitry with a transformer as the principle isolation barrier. An analogue-to-digital converter (ADC) digitises the output voltage \( V_o \) on the secondary side. The secondary side communication module encodes this value and uses opto-couplers to transmit it over the isolation barrier. The primary side communication module receives and decodes the value and provides it to the loop controller module. The loop controller is implemented as a hardware PID-controller. A Digital Pulse Width Modulator (DPWM) generates the switching signals for the primary side power stage, which stabilizes the secondary side output voltage \( V_o \).

The novel features of this approach are:

- The primary side controller can determine instant when the ADC samples the \( V_o \). This allows sampling of a settled output. The start of the received data package triggers the ADC sampling process.
- The secondary side uses the encoded data to adjust a programmable reference voltage to produce the selected \( V_o \).
- Both sides can send auxiliary data to the opposite side. This data is appended to the main data. This auxiliary data may include safety signals like over-voltage-protection (OVP), over-temperature-protection (OTP) and power failure (PF) but also arbitrary end-user data.

B. Communication System

The communication modules allow the bi-directional data link between the primary and secondary side of the SMPS. The communication modules (fig. 3) consist of:

- Interfaces to external modules, i.e. DSP, Reference, ADC and auxiliary signals. The interface models synchronise incoming asynchronous signals and ensure proper I/O timing e.g. reading ADC value when valid.
- Serial Data receiver and transmitter circuits.

By serially encoding the data for transmission the bi-directional communication system only requires two opto-couplers or equivalent devices for communication of all signals. Synchronisation of primary and secondary side occurs by recovery of the primary side clock from the received data.

The transceiver modules contain the data transmitter and receiver. These are implemented by serial shift registers and en-/decoders and contain additional sub-modules for timing and error handling. The Primary-to-Secondary and Secondary to Primary transceiver are shown in Fig. 4. and Fig 5 respectively. They are implemented using similar circuitry but differ significantly in number and direction of interface signals. The serial transmission scheme operates with use of data packages. These packages contain the following information:

- Sampling time instant controls
- Digital representation of the reference voltage value \( V_{ref} \) which determines the nominal output voltage.
- Package number, to synchronise package frames on both sides.
- Auxiliary data signals (e.g. “power loss detected”).

These signals are transmitted in encoded form together with forward error correction and protocol bits. The use of packet frames and numbers allows bits for quasi-static signals such as reference voltage value to be transmitted at a slower rate over several packages. The outgoing secondary-to-primary packages are sent synchronously to the primary side clock. This allows the primary side receiver to sample secondary data without need for synchronisation. The secondary side packets contain the ADC value and other auxiliary signals.

![Figure 3. Bi-Directional Data Transmission Scheme](image)

![Figure 4. Primary Side Transceiver](image)
C. Transmission of Sample Time instant

Of critical importance in the design of digital controlled SMPCs is control of the sampling instant of the ADC. The primary side loop controller contains a DPWM which produces a signal that controls the primary side switches (fig. 6). The rising and falling edges of this signal cause the switches to turn ON/OFF. This produces a transient disturbance on the secondary side output \( V_0 \). The ADC sampling instant should be controlled to avoid sampling during a transient disturbance. The optimal sampling instant occurs midway between the rise and fall of the DPWM signal. This information is known a priori by the primary side loop controller. The ADC sample timing information cannot be encoded as digital data, e.g. as number, because the transmission latency is too long. The solution to this problem is to “encode” the sampling time instant by using it as a trigger for the sending of the primary side-to-secondary side package. The transmitter starts to send the package when the loop controller gives the signal for the ADC to sample. The secondary side receiver then triggers the ADC when it detects the incoming package. The loop controller can compensate for latency between transmitter and receiver by advancing timing of the data packet.

D. Control System.

A fourth-order digital controller was developed for a Zero-Order-Hold representation of the small-signal transfer function of the power converter, using a generalized model predictive control method [5]. Fig. 7 compares the open loop response of the power converter and the transfer function used in Matlab/Simulink for controller development. The controller was initially designed and tested for a standard unity feedback control configuration before implementation. The digital controller, \( K(z) \), was designed to accommodate a unit delay in the control loop and includes an integrator, necessary to eliminate any steady-state error in the output response.

\[
K(z) = \frac{37.47z^4 - 68.8z^3 + 32.05z^2 - 42.25z}{z^4 - 0.4225z^3 - 0.286z^2 - 0.2915z}
\]  

III. IMPLEMENTATION

To implement the system of section II, a prototype board has been developed which includes an isolation transformer and the full primary and secondary SMPS circuitry. The ADC function is implemented using a discrete ADC. The programmable reference voltage is achieved using a bandgap voltage reference and DAC (Digital to Analog Converter). The prototype board also contains opto couplers for bi-directional data transmission. The digital communication modules and digital controller are implemented on Field Programmable Gate Array (FPGA) development boards, which are connected to the prototype board. The full prototype demonstration board is shown in Fig. 7.
IV. RESULTS

To be completed for final camera ready paper. Will include 1 figure showing power regulation. (Fig 8.)

V. SUMMARY

The paper has presented a digitally controlled isolated power converter with a bi-directional data transmission scheme. The use of a digital transmission scheme avoids the effect of opto-coupler aging on analog transmission of data and consequently overall controller performance is improved. The presented scheme allows the use of the minimum number of isolation barrier components: Only two opto-couplers are required to handle multiple signals No extra channels are required for clock information.

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