Dithered Multi-Bit Sigma-Delta Modulator Based DPWM for DC-DC Converters

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***Abstract*—Multi-bit sigma-delta based digital pulse width modulators (DPWM) are used in the control of DC-DC converters in order to achieve high resolution and therefore high output voltage accuracy at switching frequencies up to multiple MHz. The standard sigma-delta modulators which have been used in these DPWMs to date generate idle tones in the applied duty cycle which result in large oscillations in the output voltage. A dithered sigma-delta modulator is instead implemented here which eliminates these oscillations in the output voltage by adding a random signal before the quantizer in the sigma-delta modulator. The power spectral density of the duty cycle produced by the dithered sigma-delta modulator based DPWM shows a reduction in the undesirable idle tones and this is also verified experimentally using a buck converter prototype.**

Keywords—sigma-delta digital pulse width modulator, idle tones, DC-DC converters, digital control

I. INTRODUCTION

The benefits of using multi-bit sigma-delta DPWMs for DC-DC converters with switching frequencies up to multiple MHz include improved resolution and low-area low-power implementation compared with simple counter based pulse width modulators [1]. Fig. 1 illustrates the sigma-delta modulator together with a core DPWM (typically a counter) applied in a power converter control loop.

A disadvantage of standard sigma-delta DPWMs is the generation of low frequency tones by the sigma-delta modulator at certain duty cycles, which can result in large oscillations in output voltage if their frequency coincides with the corner frequency of the converter [2]. These idle tones occur for fixed duty cycle inputs, i.e. when the converter is in steady state. The low frequency tones can be significantly reduced by using a second or third order rather than a first order sigma-delta modulator [3]. Multi-stage noise shaping (MASH) modulators are also used instead of higher order modulators because stability analysis is easier for the former [4]. To ensure that the idle tones are kept at high frequencies away from the corner frequency of the converter, the difference between the resolution of the core DPWM and the input resolution must be minimized when designing the DPWM [2], at the cost of using a higher resolution core DPWM which has a negative effect on power consumption.

An alternative solution is implemented here for the multi-bit sigma-delta based DPWM which involves adding dither to the modulator loop so that the noise power of the tones is distributed at higher frequencies. This method is widely used to suppress the effect of idle tones in sigma-delta data converters [5] and has also been used in sigma-delta modulators for variable switching frequency DC-DC converters [6-7] but not for fixed switching frequency converters.

II. DITHERED MULTI-BIT SIGMA-DELTA MODULATOR BASED DPWM

A. Principle of Operation

The standard sigma-delta based DPWM has a two-stage structure consisting of the sigma-delta modulator and the core DPWM. The modulator includes a quantizer, which may be simply a truncator that removes the least significant bits, and a filter. The filter processes the quantization noise which is the difference between the input and output of the quantizer and has a transfer function given by:

$$1 - NTF(z), \tag{1}$$

where $NTF(z)$ is the noise transfer function of the modulator. The filter shapes the quantization noise so that most of the noise power is moved to high frequencies. Higher order modulators move more of the quantization noise to higher frequencies at the expense of additional complexity. Equations (2) and (3) are the noise transfer functions of first and second order modulators respectively:

$$1 - z^{-1}, \tag{2}$$

$$(1 - z^{-1})^{2}. \tag{3}$$

The minimum frequency idle tone produced by a sigma-delta based DPWM is given by:

$$f_{min\_tone} = \frac{f_{SW}}{2^{(N_H - N_{CORE})}} \tag{4}$$

where N_H is the resolution of the duty cycle input to the DPWM, N_{CORE} is the resolution of the duty cycle input to the core DPWM (D_{CORE}) and f_{SW} is the switching frequency of the power converter.

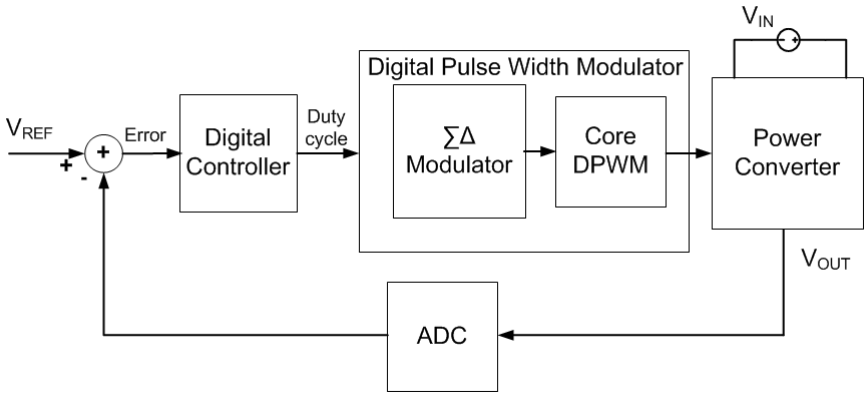

Fig. 1. Digitally controlled power converter with sigma-delta modulator based DPWM.

The proposed sigma-delta modulator includes an additional input, the dither signal, which is a pseudo random number sequence. This signal is added into the modulator loop before the quantizer [5] as illustrated in Fig. 2 of the second order modulator, which has an error feedback structure. The dither signal can be applied to a modulator of any order to minimize the effect of idle tones, for example a first order modulator with dither could be used as an alternative to a second order modulator. The dither has the effect of distributing the noise power of the idle tones across a wider frequency range, thus preventing a peak in the passband or at the corner frequency of the power converter's output filter, which is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

for a buck converter, where *L* is the inductor value and *C* is the output capacitance. A dither signal with an amplitude of one least significant bit (LSB) may be used, though the choice of the amplitude of the dither impacts the amplitude of the output voltage ripple and is a trade-off between the amplitude of the peak output switching ripple and the suppression of the idle tones. An optimal amplitude for a given case may be determined via simulation.

B. Implementation Details

The cost of implementation of the dithered sigma-delta modulator can be evaluated by examining the additional hardware block requirements compared with a standard sigma-delta modulator. A pseudo-random number generator (PRNG) is required to generate the dither signal and an adder is required to sum the dither signal with the saturated input-feedback sum. The PRNG can be implemented with a linear feedback shift register clocked at the switching frequency and a small number of logic gates. This does not represent a significant proportion of the overall size of a digital controller IC and does not consume significant additional power, especially when compared with the power consumption of the core DPWM. Alternatively if a PRNG was already used elsewhere in the IC, it could be shared to implement the required functionality in the DPWM.

III. VERIFICATION

The proposed dithered multi-bit sigma-delta DPWM has been implemented on an FPGA and applied to a 500 kHz, 20W, buck converter with a corner frequency of 8 kHz using a configuration similar to that illustrated in Fig. 1. Both first order and second order dithered modulators were implemented and they were combined with a 5-bit counter based core DPWM with trailing-edge modulation. The dithered sigma-delta modulator could have been alternatively combined with a delay line based core DPWM or some other low-power core DPWM architecture. A 12-bit high resolution duty cycle was applied to the input of the sigma-delta modulator.

A number of simulations were carried out prior to experimental analysis. Fig. 3 illustrates the power spectral density (PSD) of the output quantization noise of the first order and second order dithered sigma-delta DPWMs and provides a relative comparison with the non-dithered first and second order modulators for the application of a worst case fixed high resolution duty cycle equal to 0.25 – 1 LSB. The spikes or idle tones are clearly evident for the non-dithered modulators while for the dithered modulators the tones have been eliminated at the expense of higher noise levels across the entire frequency range. Fig. 4 illustrates how varying the dither amplitude from 1/16 LSB to 1 LSB for the second order sigma-delta modulator affects the PSD. There is still some peaking visible, particularly at low frequencies, for modulators with low amplitude dither while the largest amplitude dither results in the highest noise levels across all frequencies. A dither amplitude of 0.5 LSB was therefore chosen for the FPGA based implementation.

The first order sigma-delta dithered and non-dithered DPWMs were first applied to the experimental buck converter. Fig. 5 illustrates the output voltage for the non-dithered version with the converter in steady state with a duty cycle of 0.25 – 1 LSB. An undesirable periodic behavior can be seen in the waveform which has a frequency of approximately 3.9 kHz. This frequency corresponds to the expected value of the minimum idle tone frequency given by (4). This behavior can be explained by examining the duty cycle value applied to the core DPWM (D_{CORE}), which is shown at the bottom of Fig. 5.

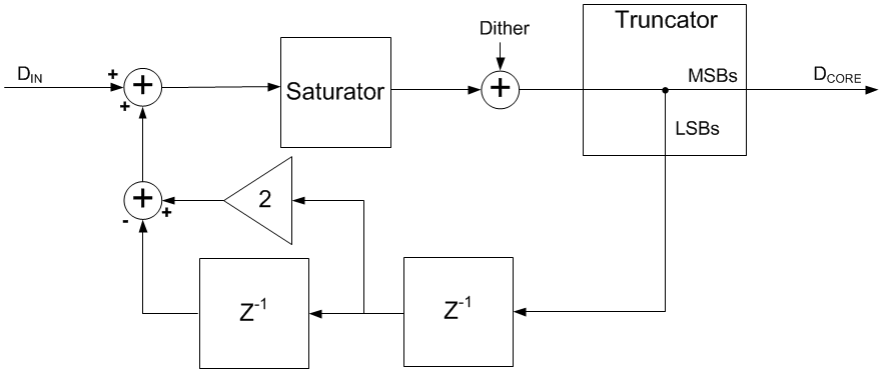

Fig. 2. Dithered second order sigma-delta modulator.

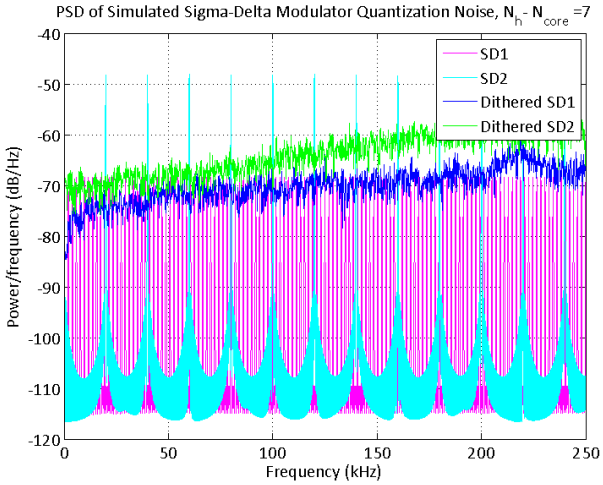

Fig. 3. Power spectral density of first and second order sigma-delta modulated duty cycle with and without dither.

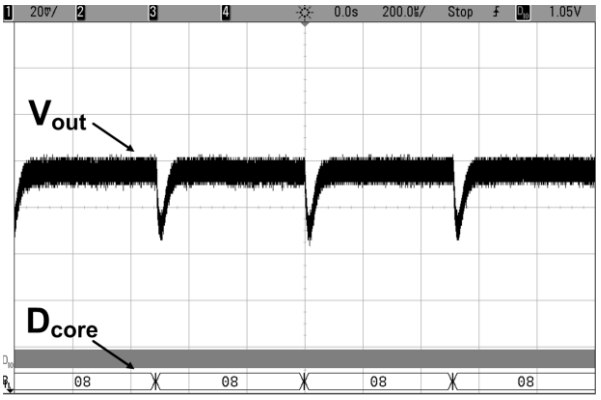

Fig. 5. Output voltage of buck converter using first order sigma-delta based DPWM.

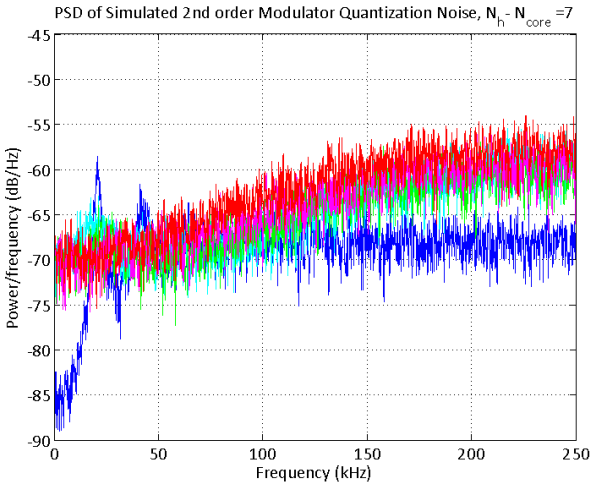

Fig. 4. Increasing dither amplitude from 1/16 LSB to 1 LSB (from blue to red) for second order dithered sigma-delta modulator.

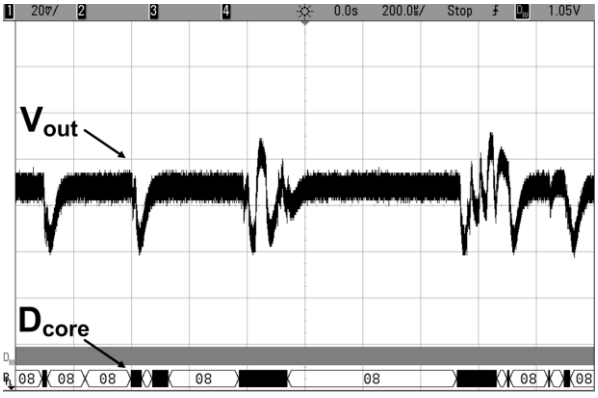

Fig. 6. Output voltage of buck converter using dithered first order sigma-delta based DPWM.

The duty cycle alternates between two values at the rate of the minimum idle tone. Fig. 6 is a scopeshot of the output voltage for the dithered first order DPWM under the same conditions.

In this case the voltage has a random pattern with more high frequency content and also a relatively insignificant increase in ripple, as expected from the simulation. The duty cycle applied

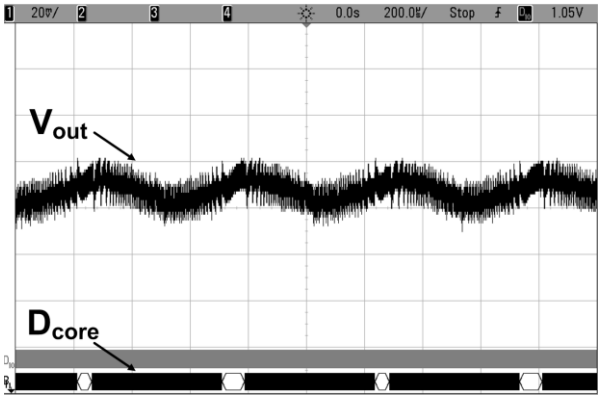

Fig. 7. Output voltage of buck converter using second order sigma-delta based DPWM.

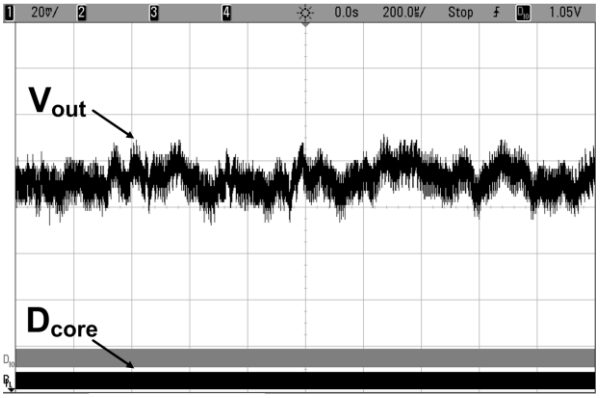

Fig. 8. Output voltage of buck converter using dithered second order sigma-delta based DPWM.

to the core DPWM changes more frequently and randomly due to the dither and thus moves the quantization noise to frequencies above the passband of the buck converter filter.

The second order non-dithered and dithered DPWMs were also applied to the experimental converter and the corresponding output voltages for the converter in steady state with a duty cycle of 0.25 – 1 LSB are illustrated in Figs. 7 and 8. Ringing can be seen in the output voltage waveform of Fig. 7, whose frequency again corresponds with the frequency of the minimum idle tone given by (4). It can be seen that the unwanted oscillations have been suppressed by the addition of the dither signal in Fig. 8. This may also be seen in the PSD plot of the output voltage noise of the buck converter in Fig. 9. The magnitudes of the most significant tones for the dithered modulator are less than those for the non-dithered modulator for the frequency range below the corner frequency of the buck converter. The dithered sigma-delta based DPWM therefore offers an alternative method to using higher order modulators in order to achieve high resolution regulation in high switching frequency power converters.

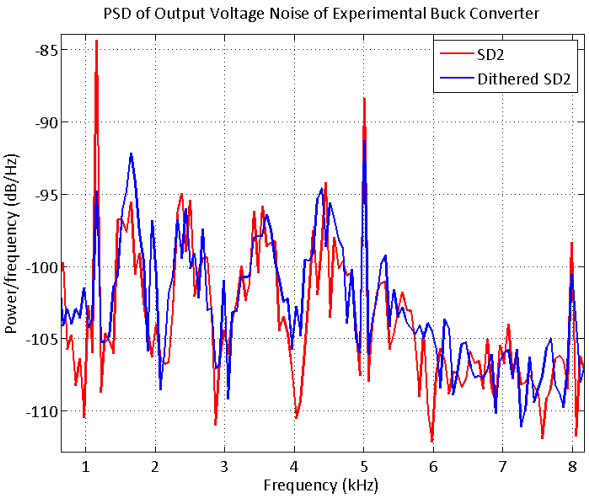

Fig. 9. Power spectral density of output voltage noise of experimental buck converter using non-dithered and dithered second order sigma-delta based DPWMs.

IV. Conclusions

Sigma-delta based DPWMs achieve high resolution in high switching frequency DC-DC converter applications. Adding dither to the sigma-delta loop can help to negate the impact of idle tones on the regulation of the output voltage. A dithered sigma-delta based DPWM has been implemented with minimal additional hardware that achieves improved output voltage performance. This also leads to potential relaxation of the requirements of the core DPWM, which has significant power consumption benefits. Trade-offs in the implementation of the dithered sigma-delta DPWM have been investigated and it has been compared with a number of other relevant sigma-delta based pulse width modulators. The use of dither in the sigma-delta loop has proved to be a viable alternative to using high order sigma-delta modulators in the DPWM.

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