Digital control law using a novel load current estimator principle for improved transient response

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Abstract—A method for the early detection of load transients using a current estimator for VR applications is presented. This technique combined with a new charge-balanced digital control law can improve the dynamic response to fast load transients. The key advantage of this new approach is the early detection of load transients which is independent of ADC sampling, where most existing solutions incorporate relatively expensive, complex and energy consuming high-speed ADCs. The presented method significantly reduces the inherent delay associated with fixed sampling detection in the control loop. The load current estimation during transient is critical for improved transient performance and allows the possibility of using a charge-balanced control law. Unlike existing algorithms, the presented control law is capable of implementing non-zero load lines required for VRMs. A full description of this control law is detailed.

The current estimator technique and the charge-balanced digital control law are critically assessed using Matlab/Simulink. The resulting transient behaviour gives a significant improvement over conventional control schemes.

I. INTRODUCTION

Transient performance and tight voltage regulations challenge today’s power controllers. In particular, the design of high-current converters, like VRMs, is dominated by the transient performance due to limited controller bandwidth and sampling delays. Several different concepts have been presented in order to overcome these issues. Most of these concepts use two different controllers: a steady-state controller which eliminates tracking errors and a transient controller which ensures fast transient recovery. A similar scheme is used in this paper (Fig. 1).

In [1], [2], “Linear–Non-Linear Control” has been presented. In this control scheme, a hysteric loop is used in parallel with a linear controller and improves the transient performance. The linear controller is not aware of the hysteric controller and this tends to lead to suboptimal results. As shown in [3], the minimum-time response on a load step is a two-action switching process, applying the optimal on/off-times. This is only possible, if accurate load current information is available. However most of today’s current sensing schemes only measure the inductor current, not the load current [4]. In order to overcome this problem, some control schemes use estimation principles to replace the load current information. For example, the capacitor current can be used as such a replacement. However it suffers from similar drawbacks.

In [5], an implementation of charged-balanced control has been presented which requires multiple current and voltage samples to calculate the control actions determined by on/off-time. For high-frequency DC-DC converters, multiple samples can only be obtained with high-speed ADCs, resulting in increased area and energy consumption.

In [6], an analogue implementation of a charge-balanced control scheme has been outlined which does not require current sensing.

In [7], a method has been presented based on the detection of the valley point during load transients. The method is designed for low-energy power converters where the equivalent series resistance (ESR) of the output capacitors is typically very small as multi-layer ceramic capacitors are used. For electrolytic capacitors (higher ESR), the method suffers from the applied approximation and would not give optimal results.

This paper details a new time-domain based current estimator approach delivering early current information during load transients utilizing a novel conversion principle. The technique can estimate the magnitude of a load step from the output voltage without introducing a significant sampling delay. To utilize this information effectively a new charge-balanced control law is introduced that is capable of implementing...
The load transient response of DC-DC converters (Fig. 2) is well analysed in literature, e.g. [9]. A typical response is shown in Fig. 3. The output voltage and current response can be obtained as a solution of a system of differential equations. Theoretically it is possible to calculate the current from the output voltage response. However it is not possible in practice to solve the governing differential equation in real-time. As an alternative approach, the solution can be approximated with the following parabola

\[ V_{\text{Out}}(t) = a(t-t_0)^2 + b(t-t_0) + c \]  

(3)

with the coefficients

\[ a = \frac{m}{2C} \] 
\[ b = R_C m - \frac{\Delta I_{\text{Load}}}{C} \] 
\[ c = V_{\text{Out}}|_{t=t_0} \]

where the converter parameters \( C \) and \( R_C \), the inductor current slew rate \( m \) and the size of the load transient \( \Delta I_{\text{Load}} \) are given. As \( b \) is the only coefficient that is function of the output current step, it can be extracted from the equation and the step size calculated.

To calculate the coefficients, \( V_{\text{Out}} \) and \( t \) in (3) are substituted with known data points \((t_n, V_{\text{Out},n})\) and the resulting system of equations is restructured to obtain \( b \). However, to solve a system of equations with three unknowns \((a,b,c)\), three data points are required. From an implementation perspective, a simpler solution would be preferred which is now derived.

Since the parameter

\[ a = \frac{m}{2C} \]  

(7)

is independent of the load transient, it can be obtained from the component values if a known inductor current slew rate \( m \) is assumed.

The inductor current slew rate for a buck converter depends on the position of the switches. It can be either \( m_1 \), if the top switch is on, or \( m_2 \), if the bottom switch is on, where

\[ m_1 = \frac{V_{\text{in}} - V_{\text{Out}}}{L} \] 
\[ m_2 = -\frac{V_{\text{Out}}}{L} \]  

(8) \hspace{1cm} (9)

As the inductor current slew rate should be constant during the estimation process, the duty cycle is saturated to 0 or 100 \%. However for multi-phase converters, a wider range of different slew rates can be obtained as a different number of top switches can be switched on at the same time. The selection of the appropriate slew rate is a matter of future research work.

If \( a \) is fixed, (3) can be solved using only two known data points \( P_1(t_1, V_{\text{Out},1}) \) and \( P_2(t_2, V_{\text{Out},2}) \). The magnitude of the load transient \( \Delta I_{\text{Load}} \) can then be calculated as

\[ \Delta I_{\text{Load}} = C R_C m + C \frac{V_1 - V_2}{t_1 - t_2} - \frac{m}{2} (t_1 + t_2) \]  

(10)

The component values used in the following sections represent the values of the equivalent single-phase converter. This simplifies the following derivations as they can be based on a single-phase converter.

\[ f_s^* = n f_{s,\text{phase}} \] 
\[ L^* = \frac{1}{n} L_{\text{phase}} \]  

(1) \hspace{1cm} (2)

Figure 2. single phase buck converter

Figure 3. Output voltage reaction on a load transient

non-zero load lines required for VRMs. The control response achieved is close to optimal. As an example, the proposed technique is demonstrated on a single-phase buck converter.

To satisfy the power needs of today processors, buck converters with multiple interleaved phases are widely used. As shown in the literature (e.g. [8]), an interleaved buck converter with \( n \) phases can be transformed into a single-phase equivalent. The inductor currents per phase are summed up (Kirchhoff’s Law) at the output capacitor resulting in a single equivalent inductor current. From this waveform, it can be shown that the inductor current slew rate \( m \) is independent of the load transient, it can be obtained from the component values if a known inductor current slew rate \( m \) is assumed.

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where the capacitance $C$, its ESR $R_C$ and the inductor current slew rate $m$ are known.

In practice, accurate knowledge of the parameters can be an issue as component values vary due to manufacturing tolerances and aging. For example for electrolytic capacitors, aging leads to smaller capacitance and higher ESR. Conversely, small ESRs (MLCC capacitors) challenge the controller design and make fast compensation difficult. The outlined current estimator works for small and high ESR capacitors as long the value is known with a certain accuracy. If the variation is too great, an auto-tuning scheme can be applied to calibrate the current estimator. This requires additional circuitry to apply a defined load on the power supply. Further research is ongoing to develop the auto-tuning methods and eliminate additional components.

Most existing conversion schemes are based on uniform sampling and measure the voltage value at defined regular time intervals. This introduces significant delays into the control loop and degenerates the control response. The approach presented in this paper is based on the measurement of time, rather than voltage. The time intervals $t_1$ and $t_2$ are measured for fixed voltage levels $V_1$ and $V_2$. If these voltage levels are chosen appropriately, the time intervals $t_1$ and $t_2$ are determined quickly. As the time is measured in the digital domain using counters, no additional conversion is required and the overall delay can be reduced significantly.

Fig. 4 illustrates how the current estimator is implemented in practice. The output voltage $V_{Out}$ of the converter contains two parts: the capacitor voltage caused by the stored charge and the voltage drop over its ESR caused by the inductor current

$$V_{Out} = R_C I_C(t) + \frac{1}{C} \int I_C(t) dt .$$

(11)

The minimisation of the detection delay using the proposed current estimator technique provides a significant advantage over conventional sensing schemes as it allows the controller to act almost instantaneously as soon as a load transient occurs. This combined with an appropriate digital control law can significantly improve the transient performance of the VRM.

Compared to conventional digital control schemes, the additional circuitry consists of comparators, counters and look-up tables. This allows a very inexpensive implementation which can easily be incorporated into existing control solutions.

III. TRANSIENT CONTROL LAW

If accurate load current information is available, a control law with load current feed forward is appropriate, e.g. “Capacitor Charge Balance” [5], [10], [11]. However existing algorithms are not able to handle non-zero load lines which are essential for VRM applications. In the following section, the basic principle is outlined first followed by the proposed load-line extension.

A. Basic Principle

Charge-balanced control is based on the replacement of the capacitor charge after a load transient with an optimal two-step operation. Fig. 5 illustrates the voltage and current waveforms for a load step. The same principle can be applied to a load drop.

With reference to Fig. 2, the output voltage $V_{Out}$ of the converter contains two parts: the capacitor voltage caused by the stored charge and the voltage drop over its ESR caused by the inductor current

$$V_{Out} = R_C I_C(t) + \frac{1}{C} \int I_C(t) dt .$$

(11)

The capacitor current equates to the difference between output current $I_{Load}$ and inductor current $I_L$.

$$I_C = I_L - I_{Load}$$

(12)
During steady-state operation the capacitor current, averaged over switching cycle, is zero keeping the output voltage constant. A load transient (a sudden change in $I_{\text{Load}}$) cannot be matched instantaneously by the inductor current, since its slew rate is limited to

\[
m_1 = \frac{dI_L}{dt} = \frac{V_{\text{in}} - V_{\text{Out}}}{L}.
\]

Therefore the capacitor current is not zero, causing a change in the stored charge and in the output voltage. This change in capacitor charge can be calculated as

\[
\Delta Q = \int I_C(t) \, dt = \int (I_L(t) - I_{\text{Load}}(t)) \, dt.
\]

With reference to Fig. 5, the area $\Delta Q_1$ can be calculated as

\[
\Delta Q_1 = T_{\text{delay}} \Delta I_{\text{Load}} + \frac{1}{2} m_1 \Delta I_{\text{Load}}^2.
\]

In order to compensate the loss in capacitor charge, the inductor current has to exceed the load current for a defined time. The resulting areas $\Delta Q_2$ and $\Delta Q_1$ in Fig. 5 are opposite in sign to $\Delta Q_1$ and are used to recharge the capacitor. They are calculated using

\[
\Delta Q_2 = \frac{1}{2} m_1 T_{\text{on,plus}}^2
\]

and

\[
\Delta Q_3 = \frac{1}{2} m_2 T_{\text{off}}^2,
\]

respectively, where

\[
m_2 = -\frac{V_{\text{out}}}{L}.
\]

If the positive and the negative areas are equivalent, such that

\[
-\Delta Q_1 = \Delta Q_2 + \Delta Q_3,
\]

then the capacitor charge has been balanced and the output voltage is restored to the reference value. To apply the control scheme, the times $T_{\text{on}}$ and $T_{\text{off}}$ can be extracted from the equations presented.

B. Load line extension

The basic algorithm is not able to incorporate a load line which is necessary for VRM applications. In this paper an approach is presented, which introduces a non-zero load line into capacitor charge-balanced control so that the algorithm is suitable for VRM applications. Incorporating a load line into charge-balanced control means that the charge of the output capacitor does not have to be restored completely. The resulting change of the voltage gives the load line response.

The difference in charge can be calculated as

\[
\Delta Q_{\text{cap}} = Q_{\text{out}} + Q_{\text{in}} = -C R_{\text{LL}} \Delta I_{\text{Load}},
\]

where $C$ is the capacitance, $R_{\text{LL}}$ the desired load line resistance and $\Delta I_{\text{Load}}$ the size of the load transient, e.g. obtained by the current estimator.

Depending on the load transient and the desired load line, $\Delta Q_{\text{cap}}$ varies in magnitude and sign.

Current profiles for the two different cases are detailed in Fig. 6 and Fig. 7, where $\Delta Q_{\text{cap}}$ is equivalent to the area between the load current and the inductor current. As the resulting charge drop may not be appropriate, this paper introduces a new time $T_b$ into the controller reaction. During this time the duty cycle is kept at its previous value, leading to a further drop in the capacitor charge. As $T_b$ is calculated using (21), it can be positive (case 1) or negative (case 2).

\[
T_b = C R_{\text{LL}} - T_{\text{delay}} - \frac{1}{2} \frac{\Delta I_{\text{Load}}}{m_1}
\]

(1): If the calculated time is positive, the saturation of the duty cycle has to be delayed for the calculated time as shown in Fig. 6. In this scenario the current-time area $T_b \Delta I_{\text{Load}}$ (shaded area in Fig. 6) is negative.

(2): If the calculated time is negative, a positive current-time area has to be added in order to compensate the capacitor’s loss in charge. Fig. 7 illustrates the current signals in this case. The required time durations $T_{\text{on,plus}}$ and $T_{\text{off}}$ can be calculated using

\[
T_{\text{on,plus}} = \frac{-2 T_b \Delta I_{\text{Load}}}{m_1 \left(1 + \frac{m_1}{m_2}\right)} \quad \text{and} \quad T_{\text{off}} = \frac{m_1 T_{\text{on,plus}}}{m_2}.
\]

IV. Simulation results

Simulations with Matlab/Simulink/PLECS verify the proposed current estimator and control algorithm. Fig. 8 and Fig. 9 show the response on a 50 A load step in comparison to a conventional digital design. The converter is a
The proposed current estimator delivers excellent results (51 A for the 50 A load step). The current information is fed into the charge-balanced control algorithm which is active during load transients. The resulting response is almost optimal and only limited by the inductor current slew rates. As shown in Fig. 8, the output voltage reaches the reference voltage when the inductor current equals the load current. After the transient control law has been executed, a steady-state control law has been executed, a steady-state linear controller intervenes and corrects any additional steady-state errors. Special care should be taken during the design of the linear controller as the controller is not permanently active. The switching between the optimal algorithm and the linear controller can lead to problems and is matter to future research.

V. CONCLUSIONS

In this paper, a new method to improve the transient behaviour of digitally controlled VRMs is presented. A novel time-domain-based current estimator is used to obtain the current information during load transients. This current information is then fed into a new control law (based on charge-balanced control) which incorporates non-zero load lines. The combination of the presented current estimator with the proposed control law can achieve transient performance close to optimal. This approach offers significant improvement over conventional control schemes without increasing the ADC sampling frequency. Future work will include the hardware implementation of the control scheme, multi-phase extension and auto-tuning techniques to increase the robustness of the system against parameter variation.

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REFERENCES


