Automatic Multi-Phase Digital Pulse Width Modulator

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Abstract—Current demands on switched-mode power supplies to deliver higher output power with improved efficiency are leading to an increased use of multi-phase power converters. With an increasing number of phases, special multi-phase digital pulse width modulators (DPWMs) prove advantageous over the parallel use of conventional DPWMs. In this paper a “smart” multi-phase DPWM is presented which incorporates a duty cycle distribution algorithm. This algorithm is based on the fastest execution of the duty cycle input command with respect to the number of switching actions per phase and switching cycle. The system provides good dynamic current sharing during transients and enables the use of “faster” digital loop compensators. Intrinsic support of a variable number of active phases (phase-shedding operation) and improved scalability over conventional designs complete the feature set. The proposed system has been implemented on an FPGA system and tested with a four-phase buck converter.

I. INTRODUCTION

With switched-mode power supplies (SMPS) moving to higher output power and smaller output voltages, the need for multi-phase power converters is continuously growing. With an increasing number of phases, the benefits of a control loop bandwidth closer to or even higher than the switching frequency of the individual phases are well-acknowledged. As simple digital pulse width modulators (DPWMs) are still used in current multi-phase designs, these tend to be one of the limiting factors of the loop bandwidth, and hence the need for improved “smart” DPWMs is clearly evident. Additionally, most of the existing architectures are not able to drive a varying number of phases which is required in systems with phase shedding operation, e.g. [1], [2].

Standard multi-phase power converter, e.g. [3], comprising of $N$ phases, use $N$ conventional DPWM modulators to generate the control signals for the power stage switches [4]–[6]. Synchronisation between the individual modulators ensures proper phase shift. Naturally sampled DPWMs update the duty cycle once per switching cycle, which allows the update of the inputs of the modulator up to $N$-times the phase switching frequency. However, each individual DPWM is only updated once per cycle leading to additional problems such as current mismatch during load transients. Most designs overcome these issues by limiting the loop bandwidth, and thereby compromising the system performance.

For single phase applications, this issue has been addressed using several different concepts, such as charged-balanced control [7], [8], linear–non–linear control [9], [10] and multi-sampled DPWMs [11]–[14]. However to date, most of these concepts have not been applied to multi-phase applications. As a consequence, multi-phase converters are still driven by standard multi-phase modulators.

Additionally, multi-phase DPWMs comprising of conventional single-phase DPWMs require synchronisation between the individual phases in order to achieve an optimal phase shift between the individual power stages. This is mandatory to gain full advantage of the parallelization of multiple phases. The phase shift is subject to the number of phases, i.e. when the number of phases changes during run-time (phase shedding), a resynchronisation is required which can lead to additional implementation requirements.

For multi-phase converters, special scalable solutions have been presented in the literature [15]–[18], which typically share area consuming hardware resources across the phases. By doing so, the design detailed in [15], [16] duplicates the same duty cycle value for all phases, and therefore restricts the implementation of current sharing techniques.

In [17], [18], an approach based on a digital-to-analogue converter architecture (DAC) is presented. The duty cycle input command is considered as an input of a DAC representing the delivered output power, which is then distributed over the individual phases. This scheme accommodates the update of the duty cycle with frequencies greater than the actual switching frequency and scales favourably with the number of phases. However, it does not support phase shedding and disrespects the number of switching actions per switching cycle and phase which can lead to an undesired increase in effective switching frequency.

In this paper, a new multi-phase DPWM scheme is presented addressing the issues outlined. It provides good hardware utilization, limits the number of switching actions per phase and cycle and supports phase shedding. The system design level is presented, followed by the proposal of the new duty cycle distribution scheme. This is followed by its implementation and verification on an FPGA.
II. SYSTEM OVERVIEW

The proposed system (Fig. 1) consists of an N-phase power stage, an analog-digital-converter (ADC), a digital loop compensator (Loop Comp), current sharing, and a “smart” DPWM modulator (AM-DPWM), incorporating a new duty cycle distribution algorithm. This algorithm is based on the fastest possible execution of the duty cycle commands while still ensuring that each phase switches only twice (on/off) per switching cycle. A dynamic number of active phases (phase shedding) is incorporated by design together with an optional sigma-delta functionality to improve the effective resolution.

III. MULTI-PHASE DPWM

A. Distribution Scheme

Before detailing the new modulation scheme, it is first necessary to understand the modulation output of conventional multi-phase DPWMs. As an example, a typical modulation output of a four-phase system is shown in Fig. 2. For each “subcycle” (Latin numbering), the duty cycle (shown below the waveform) is applied to the currently active DPWM. While the system restricts the number of switching operations per cycle intrinsically, the delay in the application of the duty cycle and the resulting distribution of the output signal are not optimal. For the given example, the phases zero ($S_0$) and three ($S_3$) take most of the transient current leading to a large current mismatch immediately after the transient. Also the delay between the reception of the duty cycle command and the application to the power stage can be up to one full DPWM cycle.

The concept of the proposed distribution scheme is based on the fastest possible execution of the duty cycle command respecting the number of allowed switching actions per phase and switching cycle. This can be quantified in the following criteria:

- Each phase is allowed to switch up to two-times per cycle (on once, off once).

Adhering to these criteria leads to a distribution of the duty cycle as shown in Fig. 3 where the standard duty cycle distribution (Fig. 2) is included for comparison purposes (shaded). As before, the duty cycle input command for each subcycle is listed in the first line below the waveform, while the second line represents the residue forwarded to the next subcycle. The arrows illustrate the redistribution of the duty cycles among the phases compared with a standard modulation scheme where the encircled number indicates the respective subcycle; only the first three redistribution steps are highlighted (in order: solid, dashed, dotted). At the start of each subcycle, the duty cycle is distributed over the currently active phases with the priority given to the phase turned on last. Only if this phase is required to be on for the entire subcycle and if the previous phase is still on, will the latter’s duty cycle be extended by the remaining duty cycle. This procedure is continued for subsequent phases.

This distribution algorithm can be expressed mathematically as

$$D_n = \begin{cases} 0, & \text{if } D_{n+1} \neq \frac{1}{N} \text{ and } i \neq 0, \\ \min \left( \frac{1}{N}, \max(0, D_k - \frac{i}{N}) \right), & \text{otherwise,} \end{cases} (1)$$

where $D_n$ is the duty cycle for each phase $n$ and time instant $k$, $D_k$ is the duty cycle input command and $i = (k + n) \mod N$. $N$ is the number of phases, which is passed to the DPWM as a parameter depending on the current operation conditions (phase shedding).
B. Implementation

The overall implementation of the proposed DPWM is based on the block diagram shown in Fig. 4. The system comprises of an input logic, one finite-state-machine (FSM) for each controlled phase, a cyclic-counter unit and a shared high-resolution DPWM module.

The input logic normalises the duty cycle input command so that the following logic blocks are independent of the current number of phases and can be implemented more efficiently. Along with a serial integer division and a modulo operation used for the normalisation, internal integral action ensures the proper application of the entire incoming duty cycle signal.

One standard high-resolution DPWM block provides the synchronization signal for the subcycle timing depending on the number of available phases and the inter-subcycle modulation for one phase if required. The cyclic-counter provides information about the current subcycle for the individual FSMs. The FSMs control the output modulation of the phases where one FSM is required per phase. Their implementation is relatively simple and independent of the number of available phases as this is handled by the input logic.

With reference to Fig. 3 and Fig. 5, each phase can be in one of three possible states:

- Off: The phase is switched off.
- On: The phase is switched on for the entire subcycle.
- Mod: The phase is modulated during the subcycle.

At the start of each subcycle, each individual FSM evaluates the current situation. Dependent on the current operation conditions, the output of the respective phase is set. It is either turned on, turned off or modulated via the auxiliary high-resolution DPWM module. This is done by a comparison of the number of currently required phases, $n_{FC}$, with a cyclic counter value, CAP, which allows a hardware effective implementation of (1).

One additional advantage of the proposed architecture is the scalability with the number of phases (Table I). Parallel single-phase DPWM (with common resynchronization logic) scale about linear with the number of phases. However, in order to achieve sufficient resolution most of today’s designs will use a hybrid architecture using analog and digital components. This increases the required area and usually involves manual layout. The proposed architecture requires digital blocks only, despite one high-resolution DPWM module, and hence is fully synthesisable. The auxiliary units require a larger initial area compared to standard DPWMs with a break-even around four phases.

IV. LOOP COMPENSATION

In order to test the performance of the proposed DPWM in closed loop operation, some additional digital blocks are required in a digital control loop (Fig. 1). Namely, a loop compensator and, due to the nature of multi-phase power converters, current sharing functionality. In the following sections, these two blocks with their system specific implementation details and requirements are described.

A. Compensator Design

Loop compensation techniques for power converters, both in the analog and the digital domain, are well-developed. A lot of research has been focused on several different techniques. For the system presented in this paper, one specific requirement has to be taken into account, i.e. the dynamic change in the number of phases. The compensator must be able to control all plants arising from a varying number of phases which results in a modification of the power converter’s transfer function.
This is caused firstly by a change of the equivalent circuit model and secondly by a change in sampling time.

For demonstration purposes, a PID-based compensator, designed using standard design techniques proves sufficient. This compensator is “retimed” for different sampling frequencies by changing its clock frequency without a change in its coefficients. This can be viewed as a modification of the compensator in the time/frequency-domain due to a change of its discretization time/frequency. The compensator remains constant in the z-domain as the coefficients are not altered. Generally speaking, a change in the sampling frequency towards lower frequencies “slows” down the compensator and moves the corner frequency to the left. Bode plots of the resulting open loop systems are shown in Fig. 6. Note that the described technique does not provide the best possible loop compensation, but proves sufficient for testing the proposed modulator. It is expected that more advanced compensation schemes, e.g. adaptive control techniques, will provide better performance.

B. Current Sharing Technique

In multi-phase power converters current sharing is a mandatory need, due to tolerances and mismatches between the individual phases. Different strategies have been investigated in the past and can be broadly categorized into two groups, i.e. active and passive techniques. Active techniques require current sensing of the individual inductor currents and distribute the current equally among the phases. Passive techniques do not require current sensing and use alternative measures to estimate the phase current. The technique employed in this paper is based on the concept detailed in [19], [20] where current sharing as a result of duty cycle matching is proposed. This balances the current among the phases based on loss minimization instead of current equalization.

To ensure duty cycle matching among the phases, several different techniques are available. However, all of them introduce additional delays into the control loop and hence degrade its performance. In this paper, a technique originally proposed for oversampled, single-phase power converters [12] is adapted to achieve passive current sharing without phase delay. A comb-filter is inserted into the system loop which rejects signals (harmonics) at multiples of the switching frequency without delaying the control loop. The bode plot of the filters transfer function is shown in Fig. 7. One advantage of the proposed method is the relatively good decoupling of the design procedures of the current sharing filter and the loop compensator.

Additionally, the proposed comb-filter (Fig. 8) is simple to implement and does not require any dedicated multipliers. Adders and shifters are sufficient in practice. Like the loop compensator, the comb-filter is retimed when the number of phases is changed. Unlike the loop compensator, the comb-filter requires some additional action during retiming.

Note when the filter is retimed with any modifications, its rejection frequencies are shifted as they are relative to the sampling frequency, e.g. \( \frac{1}{2} f_{sa} \) and \( \frac{3}{2} f_{sa} \). However, in order to ensure proper current distribution, the rejection bands need to match the switching frequency and its harmonics. While four, two and one phase operation can be covered by one filter for harmonics at \( \frac{1}{2} f_{sa} \) and \( \frac{3}{2} f_{sa} \), different rejection bands are required for three phase operation. For this case, the harmonics are at \( \frac{1}{2} f_{sa} \) and \( \frac{5}{2} f_{sa} \). Subsequently, a small modification of the comb-filter from fourth-order into a third-order system is required to move the rejection bands into the correct positions. With reference to Fig. 8, this is achieved with five multiplexers and one additional gain stage (1/3). When the multiplexer control signal, \( T \), is set to one, the filter is in third-order mode, otherwise it is in fourth-order mode.
V. VERIFICATION

A four-phase buck converter with 500 kHz switching frequency per phase has been built to prove the concept in practice. The full technical details are given in Table II.

In Fig. 9 and Fig. 10, the system’s voltage response to a 70 A load transient is shown. Fig. 11 shows the response for a system using a standard DPWM for comparison. In Fig. 11 and Fig. 9, the respective output voltage is shown (blue), together with two of the four phase currents (yellow and magenta). Note that the large noise spikes are due to pure HF-coupling of the measurement probe. In Fig. 10, the respective digital control signals (DPWMs outputs) are shown, together with the output voltage as reference signal. Also the outputs of the standard DPWM ($D_{12} \text{ to } D_{15}$) and the new modulator ($D_8 \text{ to } D_{11}$) are both shown in the same diagram, where only the latter set is used as switch control signals.

Using the new distribution algorithm, the transient response is improved by almost 40% compared to regular DPWMs. The maximum deviation is significantly reduced which is also due to an increase in the maximum loop gain. In this prototype, the gain of the standard DPWM loop is reduced by a factor of two compared with the new modulator, as a higher gain would cause a significant output voltage overshoot.

In Fig. 12, the behaviour of the DPWM during a phase shedding operation is shown. The number of phases is changed from three to four via an external control signal ($D_7$). The respective phase ($D_{15}$) is switched from tri-state mode into standard operation. At the same time, the phases are realigned with a phase shift of 90°. The phase shedding procedure does not cause any perturbation of the output voltage due to the internal distribution scheme. Note that in Fig. 12 (output voltage resolution 20mV/DIV), the unexpected increase in ripple voltage during the change in the number of phases is caused by the switching noise of the just-enabled phase as this is the nearest to the measurement probe.

VI. CONCLUSIONS

A new multi-phase DPWM modulation scheme has been presented based on the fastest possible distribution of the duty cycle input command to the power stage with respect to the number of allowed switching actions per cycle. Utilizing a new distribution algorithm, the system provides superior transient performance and inductor current distribution over systems using conventional modulators. The proposed modulator has been implemented in an FPGA prototype and its performance assessed for a four-phase buck converter. Results presented show clear advantages of the proposed system over standard DPWM modulators with a maximum performance increase of approx. 40%.

ACKNOWLEDGMENT

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Table II

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<th>Technical Details of the Prototype System.</th>
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<td><strong>Output voltage</strong></td>
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