A Novel Pole–Zero Compensation Scheme Using Unbalanced Differential Pairs

Adrian P. Ryan, *Member, IEEE,* and Oliver McCarthy

***Abstract*—The main problem in extending continuous-time filtering to higher frequencies is the sensitivity of high-frequency filters to analog integrator nonidealities such as finite dc gain and parasitic poles. The use of a cascode stage introduces internal nodes, and hence a nondominant pole, in the signal path. This has been overcome using a novel phase compensation scheme which does not require tuning of the compensating element, and is itself unaffected by tuning of the integrator's unity-gain frequency or quality factor. The scheme is based upon a MOS version of the "multi-tanh principle" where the linear range of a transconductor is divided between at least two unbalanced differential pairs operating in parallel. The common-source node of an unbalanced differential pair is not ac ground and the associated pole–zero pair may be harnessed to cancel the parasitic pole introduced by the cascode stage. The feasibility of the proposed design was evaluated with the fabrication of a test-chip on a 0.25 μm 2.5 V standard digital CMOS process. Measurements confirm that the group delay response is flat ($\pm 2\%$) over a five octave frequency range (3.5–112 MHz or 0.058–1.87f_c).**

***Index Terms*—Analog circuits, compensation, continuous time filters, differential amplifiers, linear-phase filters, multi-tanh, pole–zero.**

I. Introduction

THE transconductor is of prime importance in continuous-time filter design since the unity-gain frequency of an integrator is directly proportional to its transconductance value. The linear range of a transconductor is directly proportional to the gate-overdrive voltage ($V_{GS}- V_T$) of its input stage assuming MOS devices operating in the saturation region. Modern low-voltage process technologies offer limited headroom to the designer, severely restricting the linear input range. In addition, high-frequency filters dictate topologies with no dominant internal nodes, low input-capacitance and large values of transconductance. However, for the same bias current, the linear range and transconductance of a transconductor are inversely proportional. Therefore, requirements for both low-voltage and high-frequency operation place an upper limit on the linear range that may be achieved.

Extending continuous-time filtering to higher frequencies poses several problems. The main problem is that the behavior of high-frequency filters is highly sensitive to analog integrator nonidealities. For a real integrator with a finite dc gain of a, the dominant pole is pushed from the origin to a frequency equal to ω_0/a, where ω_0 is the unity-gain frequency of the integrator. There may also be one or more high-frequency nondominant poles. The finite dc gain results in a phase lead at the unity-gain frequency while the nondominant poles cause a phase lag (Fig. 1). The quality factor of the real integrator, assuming that all the nondominant poles p_i are at a much higher frequency than the integrator unity-gain frequency, is given by [1]

$$\frac{1}{Q_{\text{integ}}} \approx \frac{1}{a} - \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i}. \tag{1}$$

The first term represents the phase lead at the unity-gain frequency while the second corresponds to the phase lag which becomes larger as ω_0 is increased.

The first term would suggest that the use of cascode output stages is mandatory. However, some implementations have avoided their use because they introduce additional nodes, and hence parasitics, in the signal path [2]–[5]. Instead, they rely on automatic tuning circuitry to control the quality factor. One approach harnesses the output impedance of a saturated transistor, which is proportional to its bias current and inversely proportional to its length, to tune Q without sacrificing the frequency response or linearity [6]–[8]. Another technique cancels the finite output conductance of a transconductor using a negative resistance load, thereby increasing its dc gain which can, in theory, be made infinite [2], [3], [5]. A slightly negative output conductance will not cause filter instability, however, because of negative feedback, loops inherently present in the biquadratic loop . Regardless, the most popular choice is the inclusion of a cascode stage (simple [9], [10], active [11], [12], folded [13], [14], telescopic [15], [16]) or a cascaded output stage such as the G_M–C op-amp [17]–[21] to improve the integrator dc gain, and attempt to cancel the associated parasitics directly.

II. Circuit Architecture

A new pole–zero compensation scheme based upon a MOS version of the "multi-tanh" principle is introduced. The "multi-tanh" principle refers to a class of linear transconductance cells, characterized by the use of parallel- or series-connected sets of bipolar differential pairs combining multiple hyperbolic tangent functions [22]. The extension to MOS implementations operating in weak inversion is obvious and straightforward although scaling effects resulting from the altered coefficient of kT/q and errors arising from back-gate bias require consideration. However, the authors know of only two reported instances which di-

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A. P. Ryan is with the Philips Research, Briarcliff Manor, NY 10510, USA (e-mail: adrianryan@ieee.org).

O. McCarthy is with the Department of Electronic and Computer Engineering, University of Limerick, Limerick, Ireland (e-mail: oliver.mccarthy@ul.ie).

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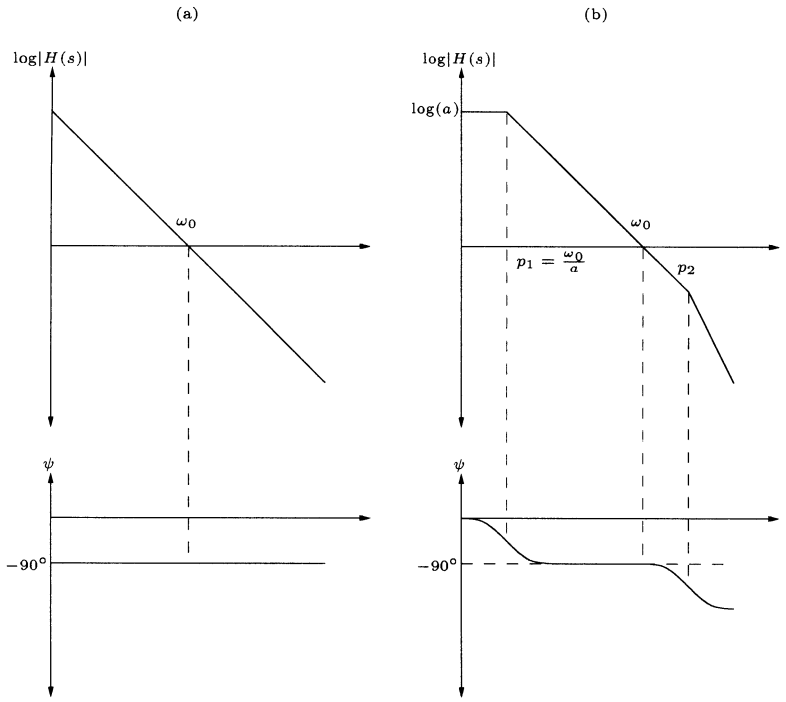

Fig. 1. (a) Magnitude and phase response of (a) ideal and a (b) real integrator.

rectly harness the square-law properties of MOS transistors for a similar purpose [23], [24] and propose the term "current-addition principle" when applying the concept to MOS process technology.

A. Linear Range and Transconductance

The multi-tanh principle is well-suited to low-voltage operation. Rather than attempt the bulk of linearization directly between the power-supplies, the burden is divided laterally between at least two, and in general N, differential pairs operating in parallel. A deliberate input offset voltage is applied to the input of each pair such that its contribution to the overall linear range of the cell is offset. Because each pair is responsible for only a fraction of the total linear range, it can be designed to provide a larger transconductance. There are several ways in which the necessary offset can be introduced. For low-order cells ($N = 2$ doublet and $N = 3$ triplet) it can be generated simply by using mismatched transistor aspect ratios. For large values of N in a bipolar technology, the offset may be introduced using bias currents operating on chains of resistors [22].

Consider the differential pair of Fig. 2 where the aspect ratio of M_1 is n times that of M_2. While this mismatch may be achieved by scaling either the width or length of the input pair, in practice both transistors have identical nonminimum gate lengths to improve device matching. For $n = 1$, the circuit reverts to the classical differential pair and will not be discussed further. However, for $n \neq 1$, the circuit is transformed into an unbalanced differential pair whose output current i_o is given by [23]

$$i_o = i_1 - i_2 = \left(\frac{n-1}{n+1}\right) I - 2\gamma k v_i^2 + \frac{\alpha}{\sqrt{n+1}}\sqrt{kI}\,v_i\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i}{2}\right)^2} \tag{2}$$

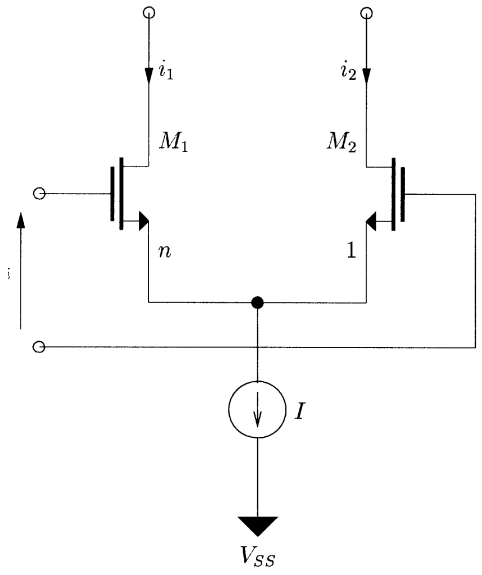

Fig. 2. Unbalanced current-biased source-coupled differential pair.

where i_1 and i_2 are the drain currents of transistors M_1 and M_2, respectively, and k is the transconductance parameter; α and γ are defined as

$$\alpha = 4\frac{n}{n+1} \quad \gamma = \frac{n}{(n+1)^2}(n-1). \tag{3}$$

It becomes apparent from (2) that a differential output current of $((n-1)/(n+1))I$ flows in an unbalanced differential pair when the applied differential input voltage is zero. In a balanced configuration, under the same operating conditions, the drain currents of the transistors which comprise the input pair are identical and, therefore, the differential output current is zero. In order to arrive at this "equilibrium position" in an unbalanced

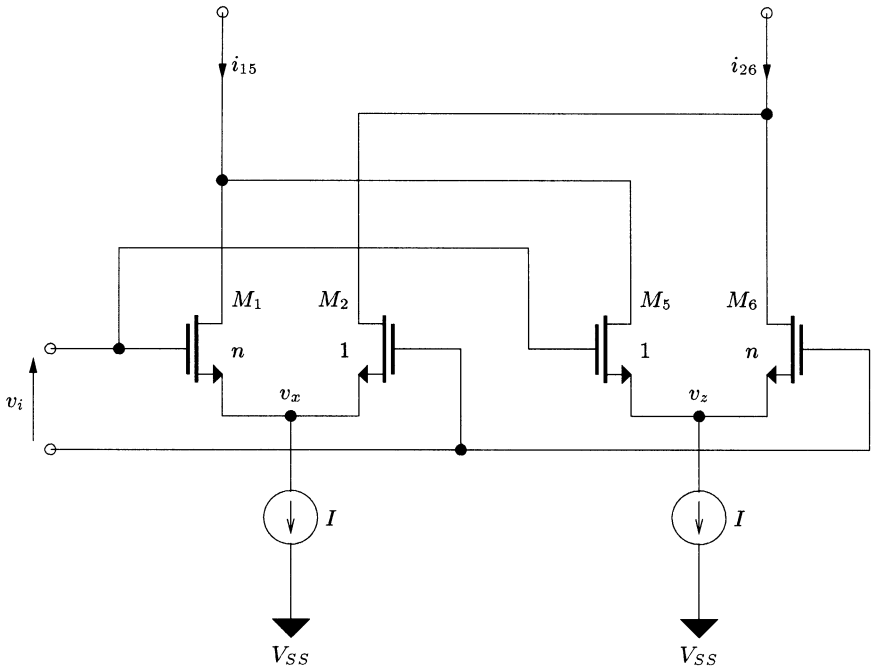

Fig. 3. Basic current-addition doublet.

structure, a negative input offset voltage must be applied (assuming $n > 1$), given by

$$v_{eq} = -\sqrt{\frac{I}{k}\left[\frac{(-1+\sqrt{n})^2}{2n}\right]}. \tag{4}$$

The differential output current of an unbalanced, or mismatched, differential pair is, therefore, an asymmetric function of the differential input voltage whose linear region is deliberately offset to accommodate negative inputs. A similar situation exists for values of $n < 1$ except that the linear range is biased to favor positive inputs. The maximum and minimum permitted values of differential input voltage (again, assuming $n > 1$) bound the range $-\sqrt{I/k} \le v_i \le \sqrt{I/(nk)}$ beyond which the circuit saturates.

Consider two parallel differential pairs $M_{1,2}$ and $M_{5,6}$ with unbalanced aspect ratios of $n:1$ and $1:n$, respectively, such that their individual asymmetric linear input ranges combine to form an extended linear range in the current-addition doublet of Fig. 3. The deliberate unbalancing of the input pairs shifts the square-law characteristic and, therefore, the associated peak transconductance of each pair away from the center of the input voltage range according to (4). It should be apparent that an optimum value of n exists for which the g_m characteristic curve is superior to that obtained using a simple differential pair. If too low, g_m will still have a peak in the middle of the input range, while if too high, g_m will sag in the middle revealing two peaks, each offset to one side. Either condition will generate third-order harmonic distortion. Using (2), the differential output current i_o is given by

$$\begin{aligned} i_o &= i_{15} - i_{26} \\ &= \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}v_i\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i}{2}\right)^2} \end{aligned} \tag{5}$$

where i_{15} and i_{26} are the combined drain currents of transistors $M_{1,5}$ and $M_{2,6}$, respectively. The transconductance may be found by differentiating i_o with respect to v_i

$$g_m = \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}\left[\frac{1-\alpha\frac{k}{I}\left(\frac{v_i^2}{2}\right)}{\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i^2}{4}\right)}}\right] \tag{6}$$

while further differentiating yields the points along the input axis corresponding to the minima and maxima of the composite transconductance function.

$$v_i = 0 \quad v_i = \pm\sqrt{\frac{I}{k}\left[\frac{3}{2}\frac{(n+1)}{n}\right]}. \tag{7}$$

In practice, the optimum value of n is determined through iterative SPICE simulation and the total harmonic distortion (THD) of the transconductor estimated for several values of n.

The current-addition triplet of Fig. 4 comprises three differential pairs with their inputs and outputs connected in parallel. The outer pairs have opposing offset ratios n, larger than for the doublet, and operate at equal tail currents. The transistors that make up the inner pair are identical so that its transconductance is centered around $v_i = 0$. This may be better understood using Fig. 5 which shows the respective transconductances of the three differential pairs and the compound transconductance. The differential output current i_o is given by

$$\begin{aligned} i_o &= i_{145} - i_{236} \\ &= \sqrt{2kI}v_i\sqrt{1-\frac{k}{I}\left(\frac{v_i^2}{2}\right)} + \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}v_i\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i^2}{4}\right)} \end{aligned} \tag{8}$$

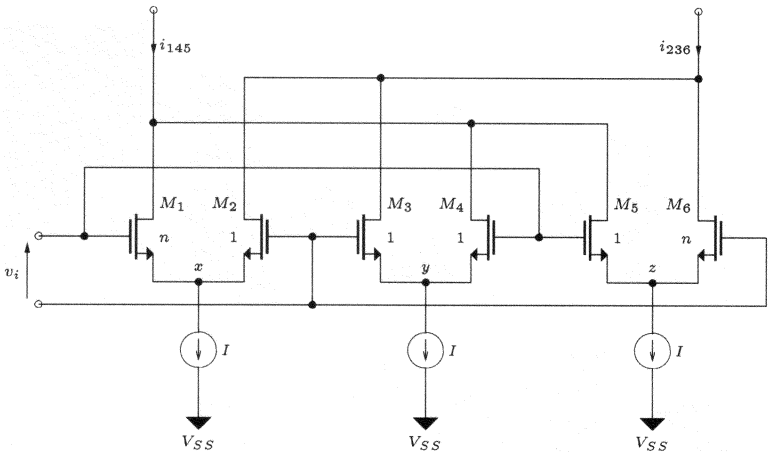

Fig. 4. Basic current-addition triplet.

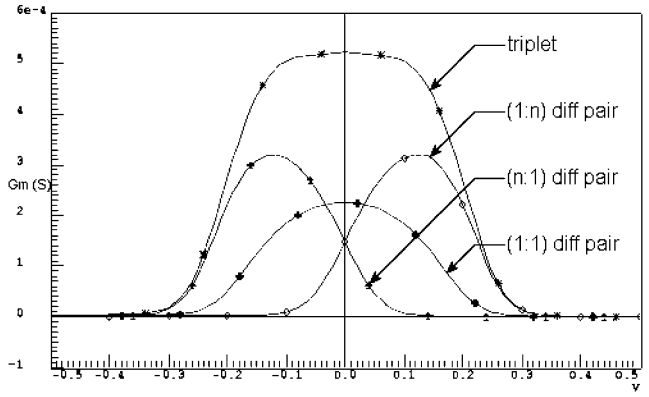

Fig. 5. Three differential pairs with input aspect ratios of $(n : 1)$, (1:1) and $(1 : n)$ are summed to form a current-addition triplet with improved linear range.

where i_{145} and i_{236} are the combined drain currents of transistors $M_{1,4,5}$ and $M_{2,3,6}$, respectively. Differentiating i_o with respect to v_i gives the small-signal transconductance

$$g_m = \sqrt{2kI}\left[\frac{1-\frac{k}{I}v_i^2}{\sqrt{1-\frac{k}{I}\left(\frac{v_i^2}{2}\right)}}\right] + \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}\left[\frac{1-\alpha\frac{k}{I}\left(\frac{v_i^2}{2}\right)}{\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i^2}{4}\right)}}\right] \tag{9}$$

which, like (8), is composed of the individual transconductance contributions of a classical differential pair with tail current I and the doublet.

B. Frequency Compensation

Consider the small-signal differential-mode half-circuit of a tunable G_M–C integrator illustrated in Fig. 6 [13]. The complete transfer function of the generalized integrator, assuming that the degeneration resistance R_ω of input transistor M_i and the resistances R_{lead}, R_{lag} and R_{comp} are zero, is given by

$$\frac{g_m}{sC_\omega}\frac{1}{1+sC_{\text{lag}}r_c} \tag{10}$$

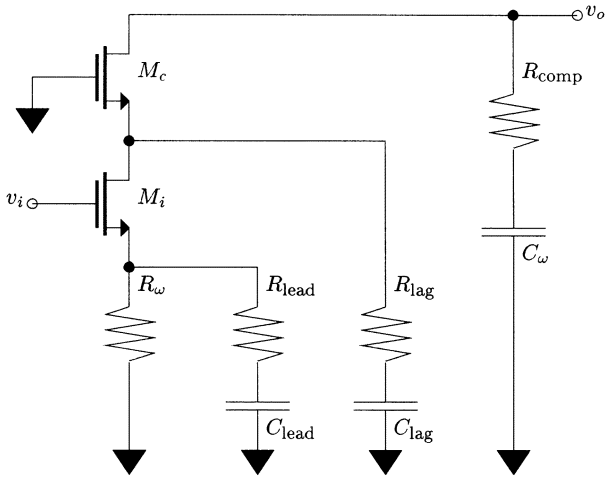

Fig. 6. Small-signal differential-mode half-circuit of tunable integrator.

where g_m is defined as the transconductance of input transistor M_i and r_c is the inverse of the small-signal transconductance of cascode transistor M_c. From (10), it is apparent that this integrator has a parasitic pole at

$$p_c = -\frac{1}{C_{\text{lag}}r_c} \tag{11}$$

in addition to the pole at dc. The phase lag introduced by the parasitic pole may be compensated by placing a resistor R_{comp} in series with the integrating capacitor C_ω [16], [25], [26]. The resulting transfer function has two poles and a single zero

$$p_0 = 0 \quad p_1 = -\frac{1}{C_{\text{lag}}r_c} \quad z_1 = -\frac{1}{C_\omega R_{\text{comp}}}. \tag{12}$$

While this first-order passive compensation may be adequate in some implementations, it is evident from (12) that the parasitic pole and zero do not track each other because the transconductance of the cascode transistor varies with process, temperature, tuning etc. In practice, R_{comp} is a variable resistance implemented using a MOS transistor operating in the triode region whose gate is driven by some form of automatic phase-tuning circuitry [11].

Up to this point, the common-source node of a differential pair was assumed to be ac ground—that is, R_ω was assumed to

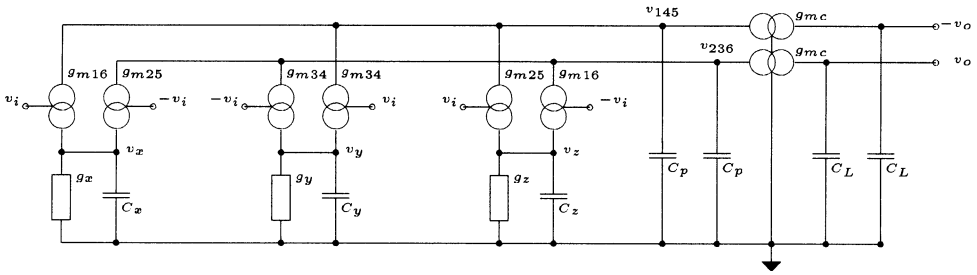

Fig. 7. Small-signal representation of the current-addition integrator.

be zero. As such, any parasitic capacitance C_{lead} present at the common-source node was effectively shorted and exerted no influence on the frequency response. Next consider the effect of source-degeneration (finite R_ω) on the integrator transfer function. Assuming R_{lead}, R_{lag} and R_{comp} are zero, source-degeneration introduces a pole–zero pair in addition to the nondominant parasitic pole of (11)

$$p_2 = -\frac{1+g_m R_\omega}{C_{\text{lead}} R_\omega} \quad z_2 = -\frac{1}{C_{\text{lead}} R_\omega}. \tag{13}$$

In this way, excess phase lag in the integrator can be corrected using the voltage-controlled degeneration resistance and the existing capacitance between the common-source node of the differential pair and ground [15], [27]. If the integrator unity-gain frequency is to be determined by controlling the differential pair tail current, then the degeneration factor must be kept low. The variable resistor may be realized with a single MOS transistor, with additional circuitry to limit the sensitivity of the resistance to the integrator common-mode input voltage. Also, because the transconductance depends not only on the bias current but the degeneration resistance as well, the combination of frequency and amplitude control loops (also known as a *vector-locked loop*) will interact. Other topologies rely heavily on source-degeneration. For example, both [14] and [28] use a digitally programmable integrator whose transconductance is determined by several parallel MOS transistors operating in the linear region. The unity-gain frequency of the integrator is tuned via the gates of these transistors. Typically, two or more of these devices are controlled with a single gate voltage while the remaining unused devices have their gates tied to the appropriate supply. In this case, the degeneration factor $g_m R_\omega$ will be quite large and the expression for the second parasitic pole can be simplified.

$$p_2 = -\frac{g_m}{C_{\text{lead}}} \quad z_2 = -\frac{1}{C_{\text{lead}} R_\omega}. \tag{14}$$

However, a problem arises because g_m changes with the programmed bandwidth while C_{lead} does not. Therefore, to obtain an integrator phase response which is largely independent of the programmed bandwidth, it is necessary to make C_{lead} track g_m. This may be achieved using several differential pairs in parallel, each with a single degeneration resistor, and connecting their output to the integrating node or to the common-mode bias voltage, as required [28].

Next, consider the proposed current-addition transconductor. Fig. 7 shows the small-signal representation of the current-addition triplet of Fig. 4 with a cascoded output stage where C_L refers to the integrating, or load, capacitance; C_p refers to the parasitic capacitance and g_{mc} refers to the transconductance of the cascode transistor. Neglecting the finite output conductance g_x and g_z of the tail current sources at nodes x and z, respectively, and assuming that v_y, the common-source node of the balanced differential pair, is ac ground, the transfer function exhibits a nondominant parasitic pole similar to that of (11) in addition to the dominant pole at dc. Also evident is a pole–zero pair introduced by the action of the unbalanced differential pairs whose common-source nodes are not ac ground [29]

$$p_3 = -\frac{g_{m16}+g_{m25}}{C_x}$$
$$z_3 = -\frac{4g_{m16}\cdot g_{m25} + g_{m34}(g_{m16}+g_{m25})}{C_x(g_{m16}+g_{m25}+g_{m34})} \tag{15}$$

where g_{m16}, g_{m25}, and g_{m34} are the transconductances of transistors $M_{1,6}$, $M_{2,5}$, and $M_{3,4}$, respectively, and $C_x(\equiv C_z)$ represents the capacitance at the common-source node of the unbalanced differential pairs. In contrast to the source-degeneration pole–zero pair of (13) and (14), in this instance both the pole and the zero are directly proportional to the transconductance and inversely proportional to C_x. Hence, they track despite variations in process, temperature and tuning. The transconductances g_{m16}, g_{m25} and g_{m34} may be further simplified and expressed in terms of a single unit transconductance

$$g_{m34} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)\left(\frac{I}{2}\right)} = \sqrt{\frac{n+1}{2}}g_m$$
$$g_{m25} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)\left(\frac{I}{n+1}\right)} = g_m$$
$$g_{m16} = \sqrt{2\mu C_{ox}\left(\frac{nW}{L}\right)\left(\frac{nI}{n+1}\right)} = ng_m. \tag{16}$$

In this implementation, the offset ratio n was chosen to be 11 for optimum linearity. Substituting this value into (15) and (16) yields

$$p_3 = -12\frac{g_m}{C_x} \quad z_3 = -5\frac{g_m}{C_x}. \tag{17}$$

It is evident from the above result that the zero dominates the response and, as such, the net phase lead of the pole–zero pair may be used to cancel the phase lag introduced by the nondominant parasitic pole of (11). Since the transconductance terms present in the numerator of the expressions for the pole–zero pair and the parasitic pole are functions of the same bias current, and capacitances C_x and C_{lag} in the denominator are composed of similar ratios of both intrinsic gate-oxide capacitance

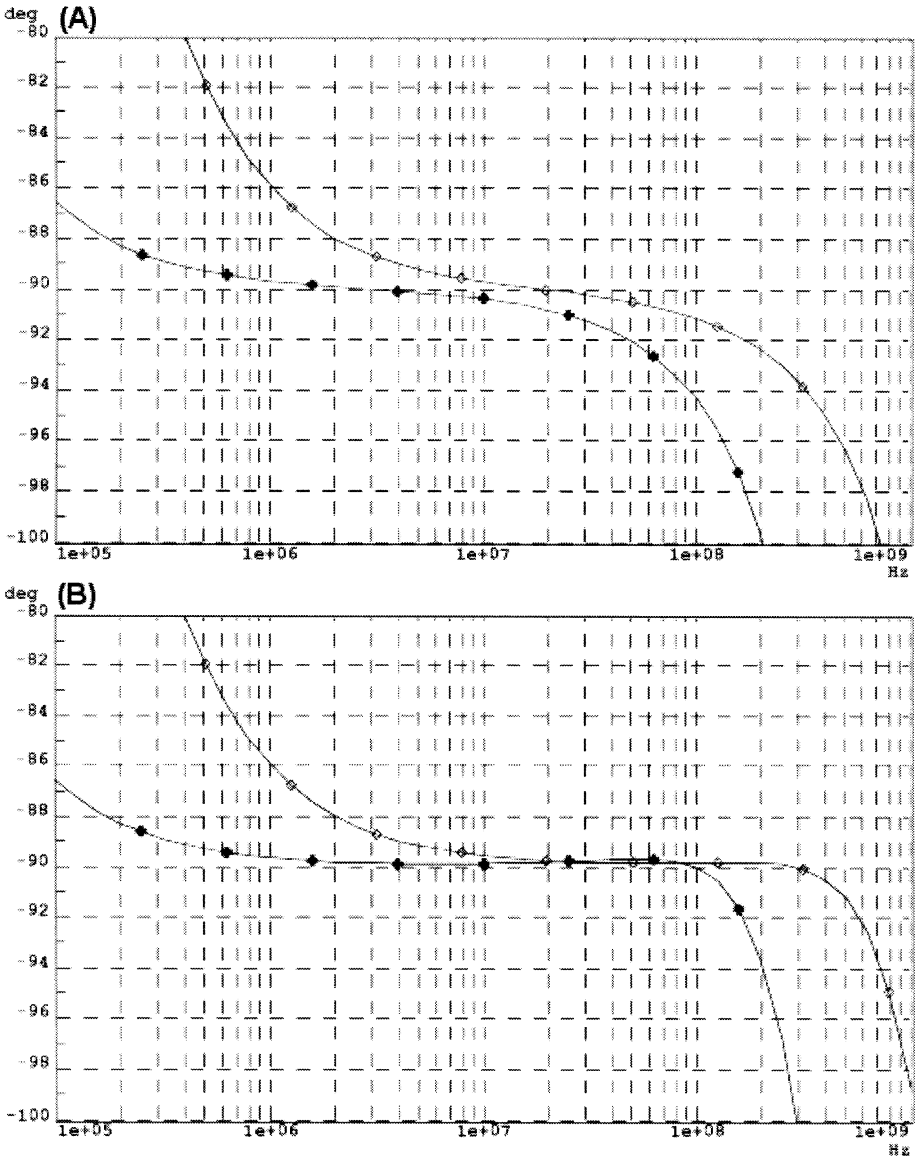

Fig. 8. Phase response of current-addition triplet at extremes of process, temperature and tuning (a) before and (b) after pole–zero compensation.

and extrinsic overlap and junction capacitances, this cancellation scheme is highly robust. This observation is confirmed by extensive computer simulation of the phase response with and without compensation at extremes of process, temperature and tuning, as shown in Fig. 8.

In practice, the offset ratio n is determined by linearity considerations while the phase error is compensated solely by adjusting the capacitance C_x and C_z present at nodes x and z, respectively. This may be accomplished with an explicit capacitor connected directly between nodes x and z, analogous to that of a capacitively-degenerated differential pair [30]. However, in this implementation, the size of the tail current source was scaled to provide the necessary value of C_x and, thus, preserve the matching of intrinsic and extrinsic capacitances that constitute both the parasitic pole and the compensating pole–zero pair.

The authors know of only one other reported phase compensation scheme which does not require tuning of the compensating element, and is itself unaffected by tuning of the integrator's unity-gain frequency or quality factor. Based on partial positive feedback, it consists of the parallel connection of two transconductors but with opposite polarity, analogous to the cross-coupled differential pair transconductor. First-order phase compensation is achieved at the expense of a reduction in the effective transconductance [31], thus making this scheme unsuitable for high-frequency filter applications. However, because the effective transconductance is given by the difference between transconductances, it has the added advantage of an extended tuning range.

C. Cascode Output Stage

The final design decision regarding the proposed transconductor is the choice of cascode output stage. Initially, a folded-cascode topology similar to that shown in Fig. 9 was considered because of its suitability for low-voltage design. However, one drawback of the folded-cascode topology is that the cascode transistor in the signal path is of a different device type to that used in the input stage. This may have implications for the pole–zero compensation scheme described earlier which relied on good matching between the transconductances of these devices.

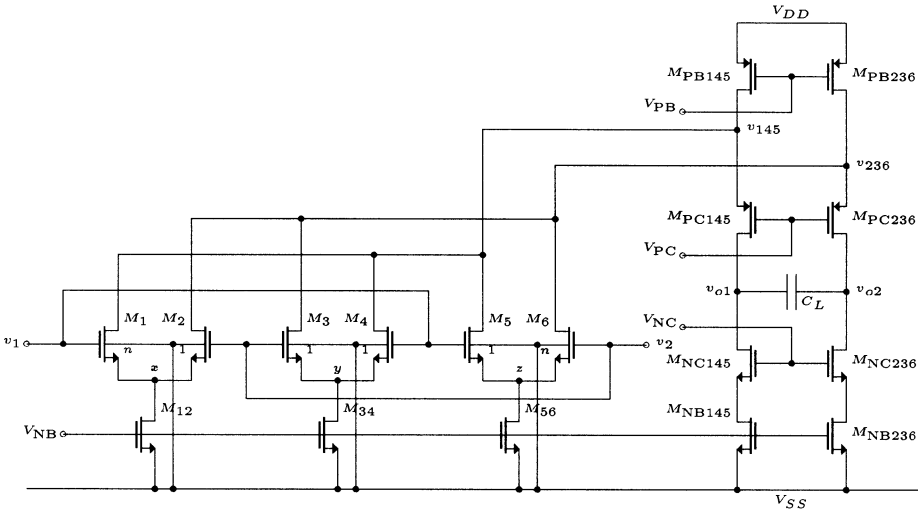

Fig. 9. Current-addition triplet with folded-cascode output stage.

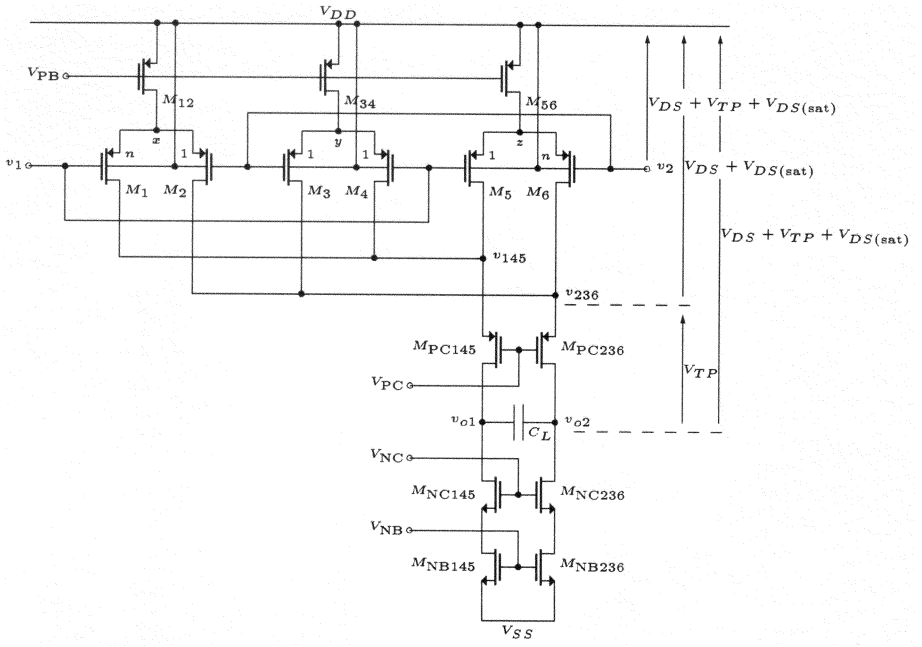

Fig. 10. Current-addition triplet with telescopic output stage.

For this reason, a telescopic output stage like that shown in Fig. 10 was used. The output of each transconductor in the biquadratic loop is connected directly to the input of the next stage—there is no level-shift circuitry. Therefore, each transconductor shares the same input and output common-mode level which is not midsupply but skewed to maximize the gate-source voltage, and therefore the linearity and tuning range, of the current-addition triplet. The choice of common-mode level means that the voltage headroom available to bias transistors M_{NB145} and M_{NB236} and cascode transistors M_{NC145} and M_{NC236} is limited, but this is of no great concern since these devices do not carry signal current and can therefore have large aspect ratios. More importantly, the input stage and its cascode transistor are composed of the same device type.

Unfortunately, the problem with using identical common-mode voltage levels at the input and output of a telescopic stage is the severe demands it places on cascode transistors M_{PC145} and M_{PC236}. The headroom available to these devices is determined by the threshold voltage of the input transistors and is compounded by the fact that the source voltages of the unbalanced differential pairs, nodes x and z in the schematic, are a function of the input signal (analogous to a source-follower) while the voltage at the integrating node is 180° out of phase.

III. Experimental Results

In order to evaluate the proposed transconductor, a fourth-order filter comprising two second-order sections connected in cascade was fabricated on a 0.25-μm 2.5-V standard digital CMOS process. Because the headroom of the cascode transistor is determined by the threshold voltage of the input stage, a PMOS-type current-addition triplet transconductor was implemented. This is due to the fact that the threshold voltage of the NMOS input stage did not offer sufficient headroom to

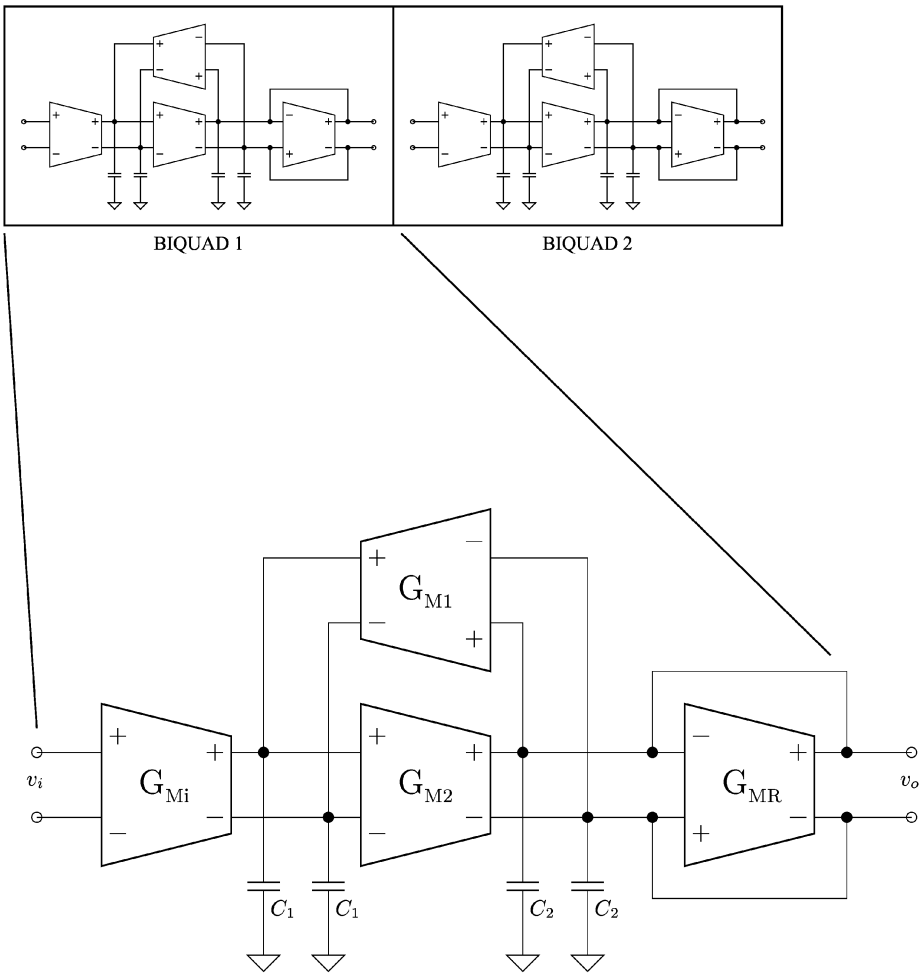

Fig. 11. Filter topology.

bias the cascode transistors and is specific to the process used. As a result, the transconductance and matching characteristics of the PMOS current-addition triplet will suffer compared to an NMOS implementation with similar device sizes.

The biquadratic topology shown in Fig. 11 was chosen primarily because of its modularity. In addition to this, statistical simulations show that such an architecture results in a reduced phase response sensitivity compared with a ladder topology. The most general form of the low-pass filter transfer function is given by

$$H(s) = H_1 \frac{\omega_1^2}{s^2 + \frac{\omega_1}{Q_1} s + \omega_1^2} \cdot H_2 \frac{\omega_2^2}{s^2 + \frac{\omega_2}{Q_2} s + \omega_2^2}. \tag{18}$$

The values for the natural frequency and Q of the individual biquads were chosen to satisfy a 0.05° equiripple-phase characteristic [32], where

$$\begin{aligned} \omega_1 &= 1.075\,213\,1 \quad Q_1 = 0.557\,280\,1 \\ \omega_2 &= 1.586\,493\,6 \quad Q_2 = 1.065\,191\,9. \end{aligned} \tag{19}$$

The biquad order was dictated by the process of minimizing transient and dc gains from the input to the integrating nodes. Specifically, the biquads are ordered according to increasing natural frequency and quality factor [10], [33]. Referring once again to Fig. 11, the transfer function of a single biquad is

$$H(s) = H_0 \frac{\frac{G_{M1}}{C_1}\frac{G_{M2}}{C_2}}{s^2 + \left(\frac{G_{MR}}{C_2}\right) s + \frac{G_{M1}}{C_1}\frac{G_{M2}}{C_2}}, \quad \text{where} \quad H_0 = \frac{G_{Mi}}{G_{M1}}. \tag{20}$$

Consequently, the biquad natural frequency and quality factor are given by

$$\omega_0 = \sqrt{\frac{G_{M1}G_{M2}}{C_1C_2}} \quad Q = \frac{\sqrt{G_{M1}G_{M2}}}{G_{MR}} \sqrt{\frac{C_2}{C_1}}. \tag{21}$$

It is evident from (21) that the natural frequency is determined by g_m/C, whereas the desired quality factor may be realized by dimensionless ratios of either capacitors or transconductors, or a combination of both. In this instance, each biquad uses the same optimal transconductance element and the integrating capacitance is varied as required

$$\omega_0 = \frac{G_M}{\sqrt{C_1C_2}} \text{ and } Q = \sqrt{\frac{C_2}{C_1}}, \quad \text{if } G_{Mi} = G_{M1} = G_{M2} = G_{MR} = G_M. \tag{22}$$

In addition, when gate-oxide capacitance is used as integrating capacitance, the intrinsic parasitic capacitance associated with the next transconductor stage may be included as part of the overall load capacitance. Because both oxide thickness and

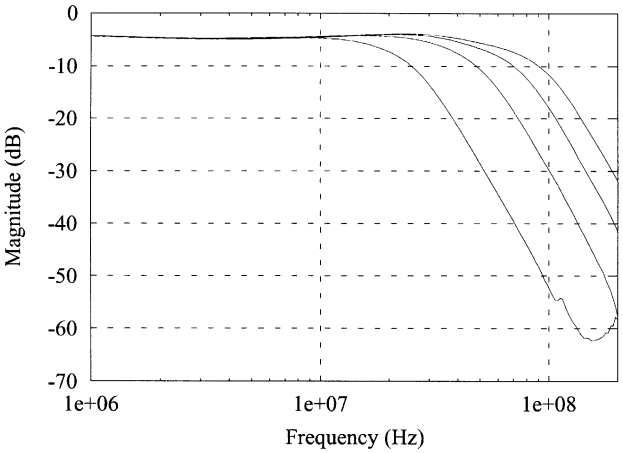

Fig. 12. Typical magnitude response at four discrete tuning levels.

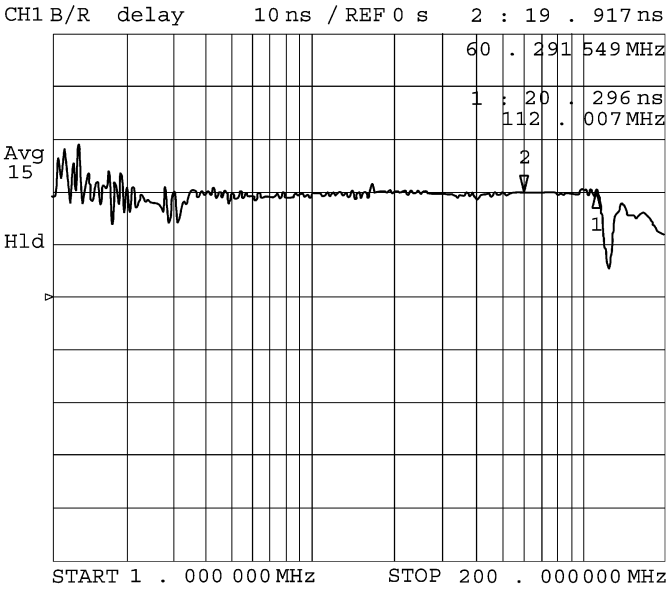

Fig. 13. Typical group delay response of filter for $f_c = 60$ MHz.

channel width appear identically in expressions for g_m and C, MOS capacitors can reduce the effect of process variation by making g_m/C insensitive to these highly-variable parameters. Thus, accurate time constants are possible, even if the filter operates exclusively on parasitic capacitances [2]. Channel length, however, will continue to contribute variability.

The small-signal characteristics of each part have been measured with a -10 dB $\cdot$ m (200 mV_{pp}) signal applied to the input stage at four discrete tuning levels. The minimum and maximum cutoff frequencies were measured to be 20 and 70 MHz, respectively as shown in Fig. 12. At the lowest cutoff-frequency, a worst-case THD of -43 dB (0.7%) was observed for an applied 3.5-MHz input sine wave.

The group delay response of the filter is shown in Fig. 13. A typical cutoff frequency of 60 MHz (marked on plot) was selected for the purpose of this analysis. Measurements confirm that the group delay response is flat ($\pm 2\%$) over a five octave frequency range (3.5–112 MHz or 0.058–1.87 f_c).

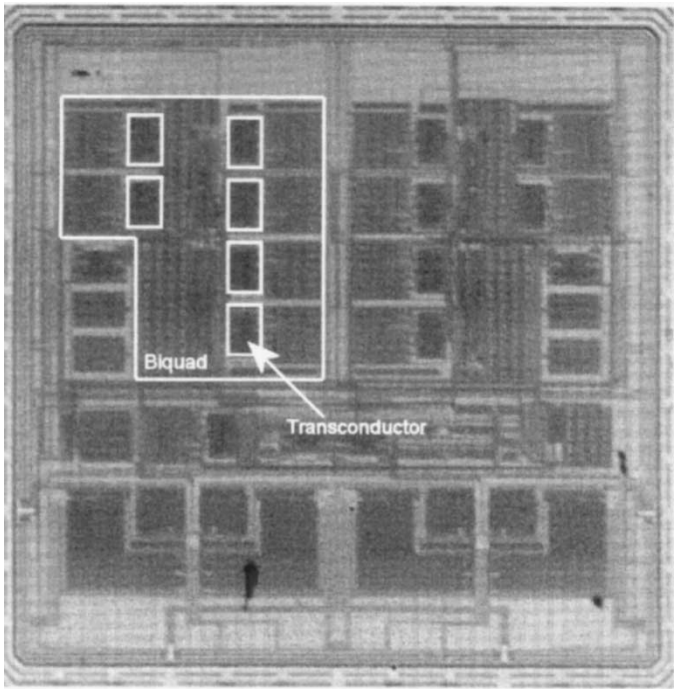

Fig. 14. Microphotograph of the chip.

A microphotograph of the prototype chip is presented in Fig. 14. The total chip area was 4.41 mm^2 and it consumed 37.5 mW from the 2.5-V supply. The filter core represents approximately 25% of the total chip area with the remainder being occupied by on-chip automatic tuning circuitry, output buffers for test purposes and the I/O ring. In addition, a high degree of programmability and redundancy was implemented in the bias and load circuits of each transconductor stage. Thus, further significant reductions in area are possible.

IV. Conclusion

A class of linear transconductance cells, based on the multi-tanh concept, has been reviewed and extended to MOS. The current-addition principle is well-suited to low-voltage operation because the burden of linearization is divided laterally amongst several parallel input stages. As such, it exhibits excellent linearity and may be tuned over a wide range of transconductance values.

Finite dc gain, in this implementation, mandates the use of a cascode stage which inevitably introduces internal nodes, and hence a nondominant parasitic pole, in the signal path. This has been overcome using a novel phase compensation scheme which does not require tuning of the compensating element, and is itself unaffected by tuning of the integrator's unity-gain frequency or quality factor. This scheme is based upon the realization that the common-source node of an unbalanced differential pair is not ac ground and harnesses the associated pole–zero pair to cancel the parasitic pole introduced by the cascode stage.

The fabrication of a test-chip was necessary to evaluate the performance of the prototype filter and its associated support circuitry. Measured results (summarized in Table I) are very encouraging. The group delay response is flat ($\pm 2\%$) over a five octave frequency range (3.5–112 MHz or 0.058–1.87 f_c).

TABLE I
SUMMARY OF FILTER SPECIFICATIONS AND MEASURED RESULTS

Filter type	0.05° equiripple-phase
Filter order	4 (two biquad. stages)
Filter topology	G_M–C
Max. cutoff frequency ($f_{c\text{MAX}}$)	70MHz
Max. tuning range	3.5:1
Group Delay ripple (range)	$< 2\%$ ($0.058f_c$–$1.87f_c$)
Max. Input Signal	200mV_{pp}
Total Harmonic Distortion (THD)	$< 0.7\%$ (-43dB)
Supply Voltage	2.5V
Power Consumption	37.5mW
Process Technology	0.25μm 2.5V CMOS
Total Chip Area	4.41mm^2

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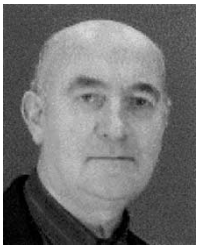
Adrian P. Ryan (S'98-M'02) was born in Tralee, Ireland in 1974. He received the B.Eng. (with honors), M.Eng. and Ph.D. degrees in electronic engineering from the University of Limerick, Limerick, Ireland in 1996, 1998 and 2001, respectively.

From 1996 to 2001, he was working in the Circuits and Systems Research Center at the University of Limerick where he designed analog CMOS filters for disk drive read-channel applications. In 2001, he joined Philips Research USA, Briarcliff Manor, NY as a Senior Member of Research Staff in the Projection Display Systems Group where he develops driver circuitry for Liquid Crystal on Silicon (LCoS) projection displays. His present interests are in the field of high-speed frequency synthesizers and internally varying analog circuits.



Oliver McCarthy received the Ph.D. degree in electrical engineering from the National University of Ireland, Cork, Ireland, in 1970.

He was a Lecturer and later a Senior Lecturer and is currently an Associate Professor of Electronic Engineering at the University of Limerick, Limerick, Ireland. His teaching and research are in the areas of analog circuit design and digital signal processing.